

# Compal Confidential

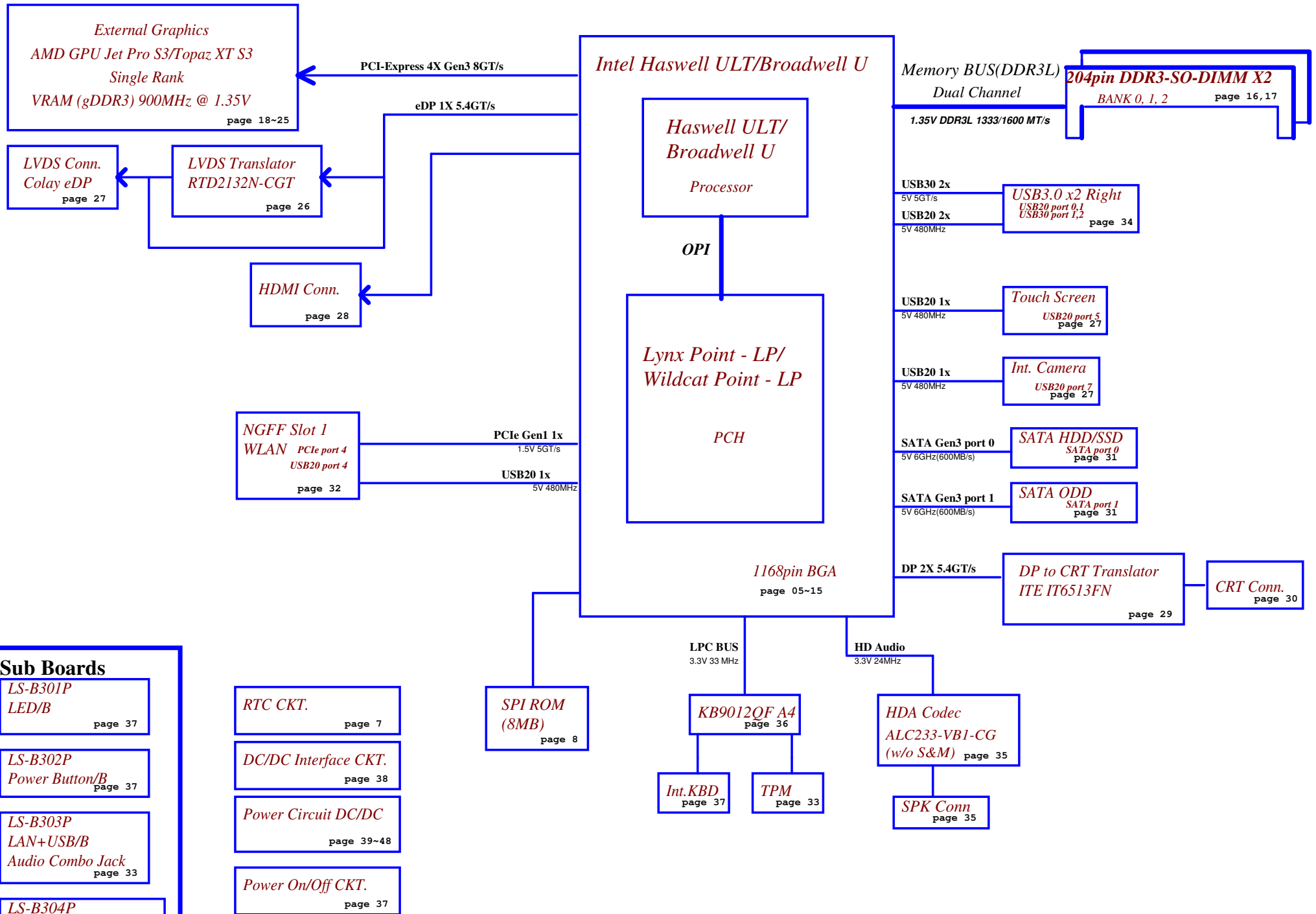
## ZSWAA/ZCWAA Schematics Document

Intel Haswell ULT/Broadwell U with DDR3L  
AMD GPU Jet Pro/Topaz XT S3 (Single Rank)

# LA-B301P REV 1.0 Schematic

Intel Processor (Haswell ULT/Broadwell U)  
2014-02-10 Rev 1.0

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## Sub Boards

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LAN+USB/B  
Audio Combo Jack  
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CardReader/TP/LID B  
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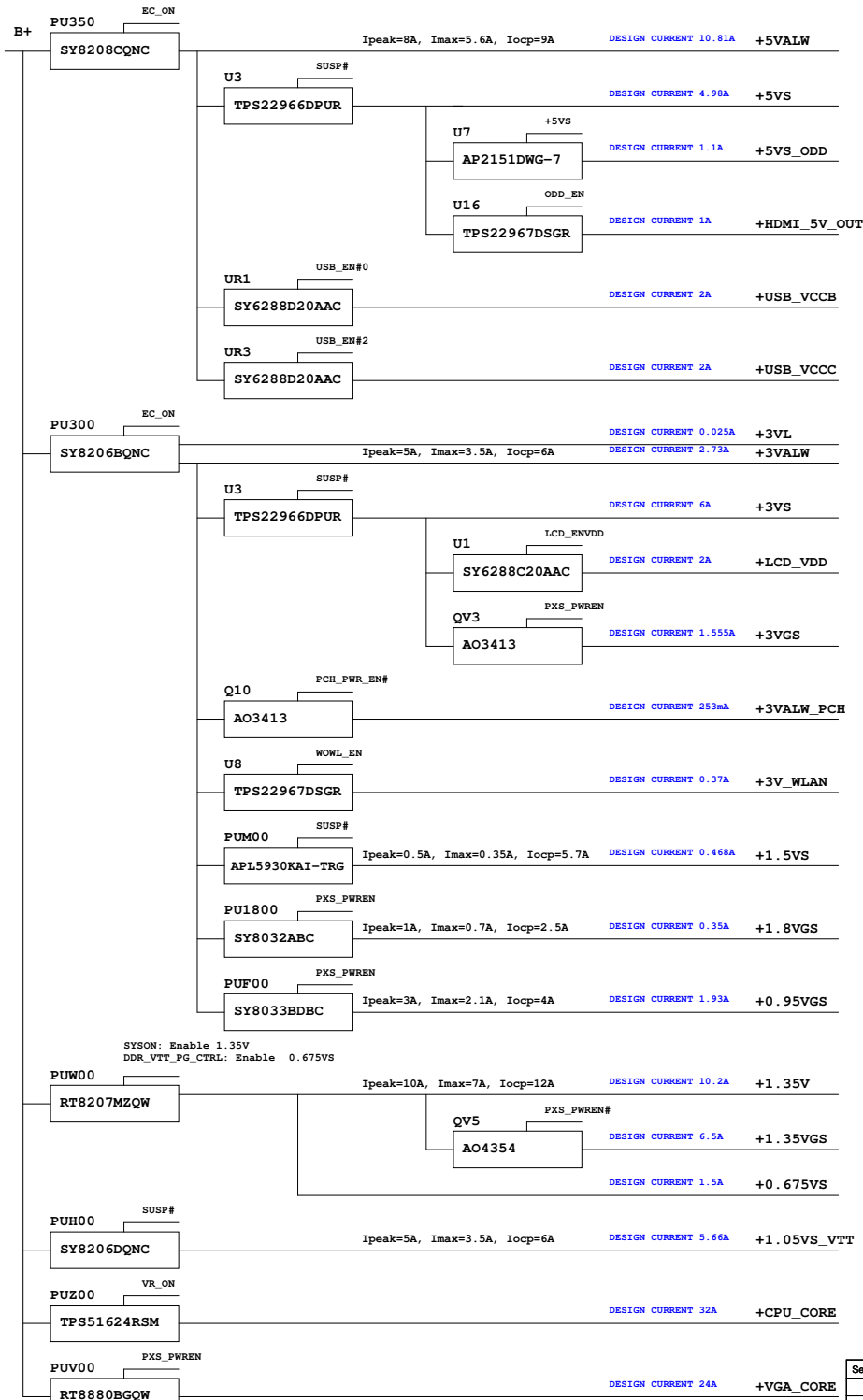
RTC CKT.  
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DC/DC Interface CKT.  
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Power Circuit DC/DC  
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Power On/Off CKT.  
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## Voltage Rails

( O MEANS ON X MEANS OFF )

power plane  State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +1.5VALW	+1.35V	+5VS +3VS +1.5VS +CPU_CORE +VGA_CORE +3VGS +1.8VGS +1.35VGS +0.95VGS +1.05VS_VTT
	S0	O	O	O	O	O
	S1	O	O	O	O	O
	S3	O	O	O	O	X
	S5 S4/AC	O	O	O	X	X
	S5 S4/ Battery only	O	O	O	X	X
	S5 S4/AC & Battery don't exist	X	X	X	X	X

## PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b

## EC SM Bus1 Address

## EC SM Bus2 Address

Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b	+3VS	PCH	96 H	1001 0110 b
+3VL	Smart Charger	12 H	0001 0010 b	+3VGS	AMD GPU	9E H	1001 1010 b
Power	Device	HEX	Address				

Platform	SKU	CPU	PCH	VGA
Intel SharkBay ULT	UMA DIS	Haswell-M ULT Processor	Lynx Point - LP	AMD GPU Jet Pro S3 Topaz XT S3

## BTO Option Table

Function	SKU		Processor		GPU		VRAM	Internal Panel		HDMI	Wake On Wireless	
Description	UMA	DIS	HASWELL	BROADWELL	JET	TOPAZ	X76	LVDS	eDP	HDMI	WOWL	NON-WOWL
Explain	UMA	DIS	HASWELL	BROADWELL	JET	TOPAZ	X76	LVDS	eDP	HDMI	WOWL	NON-WOWL
BTO	UMA@	VGA@	HASWELL@	BROADWELL@	JET@	TOPAZ@	X76@	LVDS@	IEDP@	HDMI@	ISCT@	NOISCT@

Function	CPU (R1 PN)					
Description	I3-4005U	I5-4200U	I3-4010U	2990U	I5-4210U	I3-4015U
Explain	SA000072Q70	SA00006SM80	SA00006SXA0	SA00007LM00	SA00007LO00	SA00007LN00
BTO	4005UR1@	4200UR1@	4010UR1@	2990UR1@	4210UR1@	4015UR1@

Function	CPU (R3 PN)		
Description	I3-4005U	I5-4200U	I3-4010U
Explain	SA000072Q60	SA00006SM90	SA00006SX90
BTO	4005UR3@	4200UR3@	4010UR3@

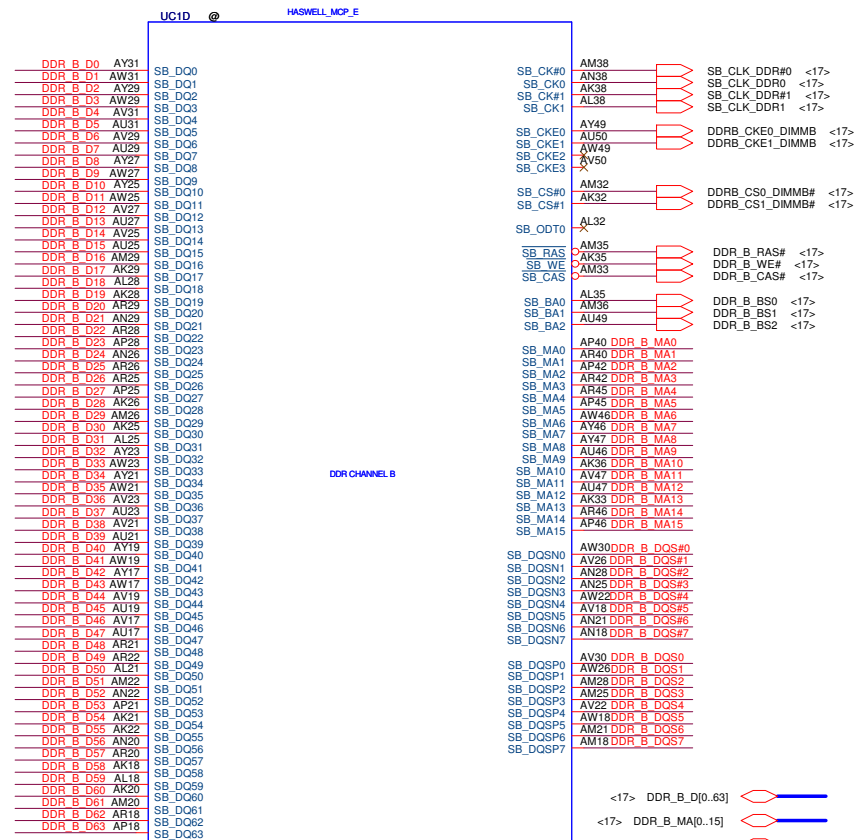
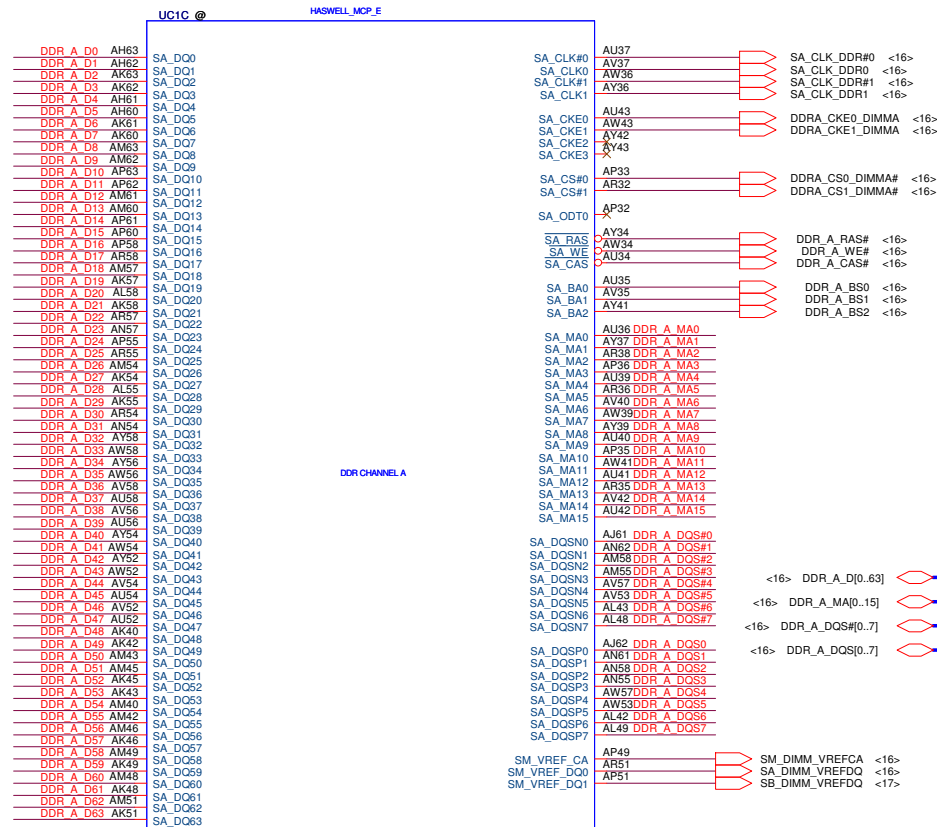
Function	ODD		XDP	FIX	Short pad	ESD
Description	ZPODD	Non-ZPODD	XDP	FIX	Short pad	ESD
Explain	Zero Power ODD	Non-Zero Power ODD	XDP	FIX	0 ohm short pad	ESD
BTO	ZPODD@	NONZP@	XDP@	FIX@	Rshort@	ESD@ @ESD@

Function	EMI		CAM_EMI		CRT_EMI		TPM_EMI		TOUCH_EMI	
Description	EMI		CAM_EMI		CRT_EMI		TPM_EMI		TOUCH_EMI	
Explain	EMI		CAM_EMI		CRT_EMI		TPM_EMI		TOUCH_EMI	
BTO	EMI@	@EMI@	CAM_EMI@	@CAM_EMI@	CRT_EMI@	@CRT_EMI@	TPM_EMI@	@TPM_EMI@	TOUCH_EMI@	@TOUCH_EMI@

STATE	SIGNAL		
	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1 (Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

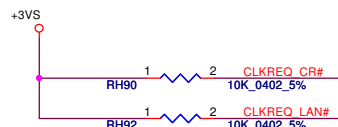
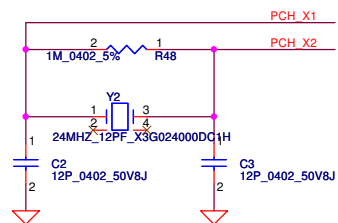
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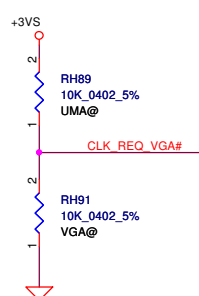


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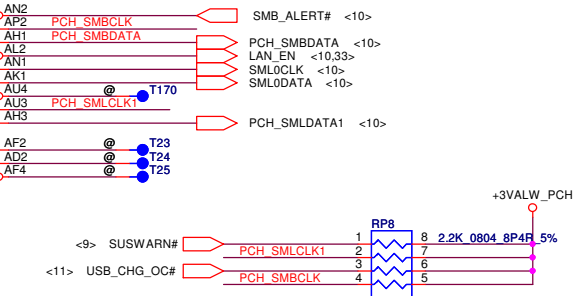
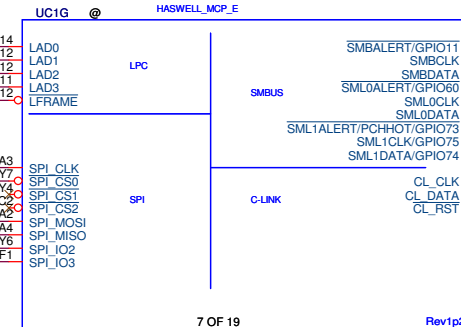
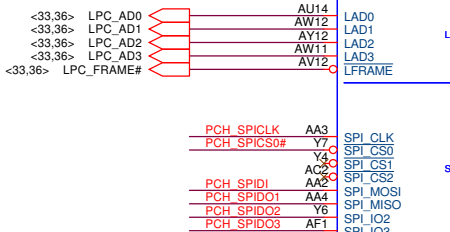
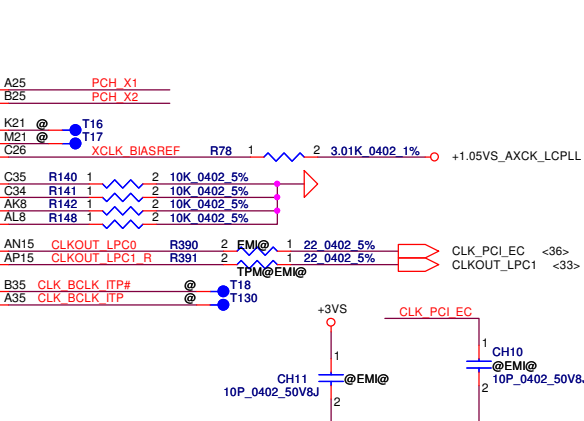
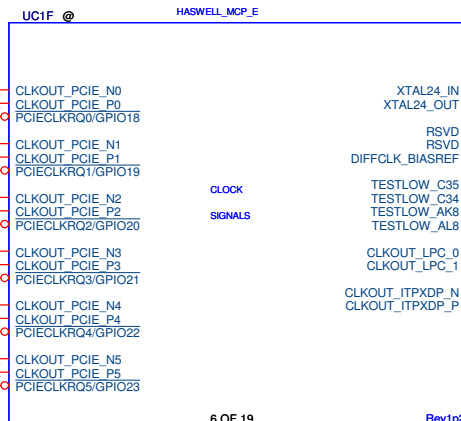


CLKREQ\_WLAN# pull high on page 10

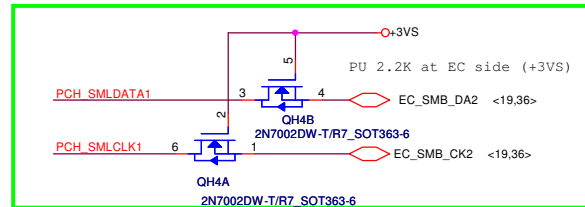
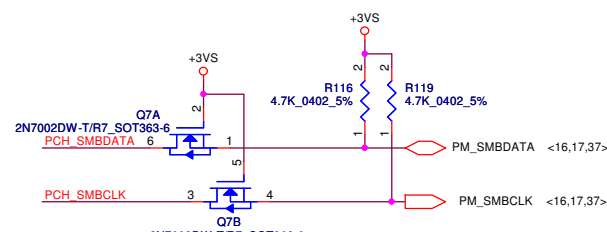
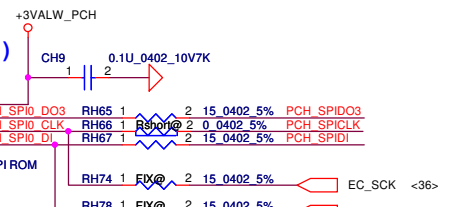


PCIE LAN

WLAN



PCH\_SMBDATA pull high on page 10



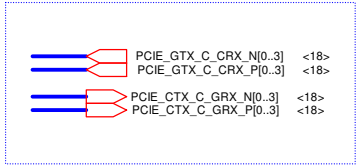
Please place UH3 close to U1 CPU,  
Please place RH66, RH67, RH68 near UH3

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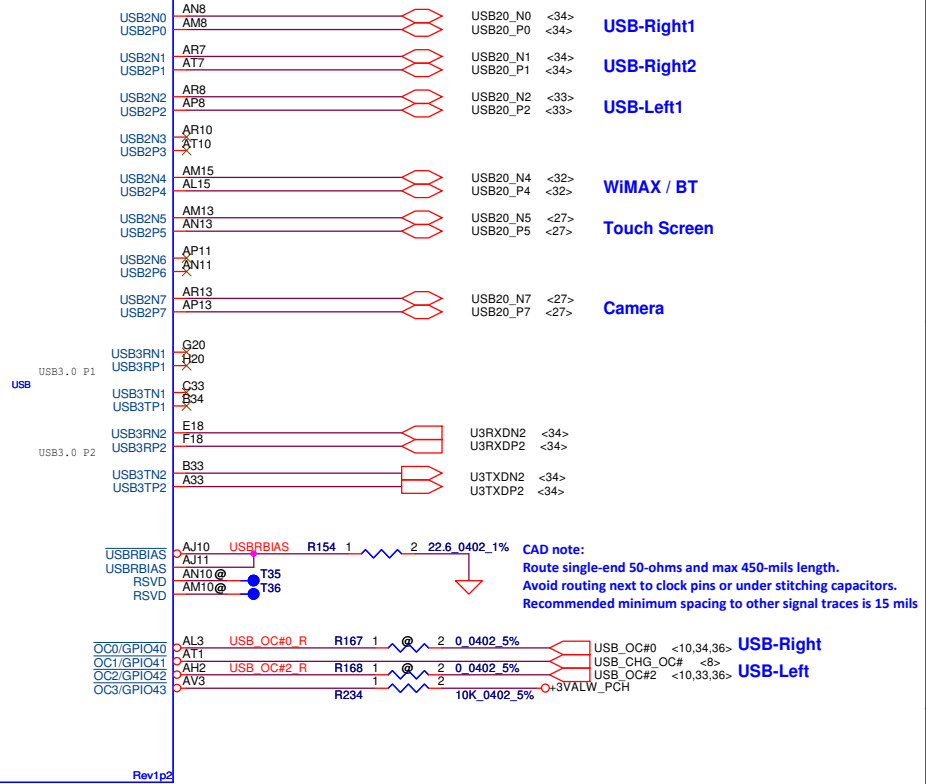
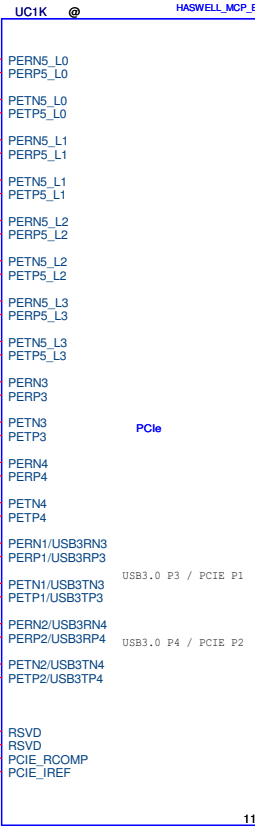
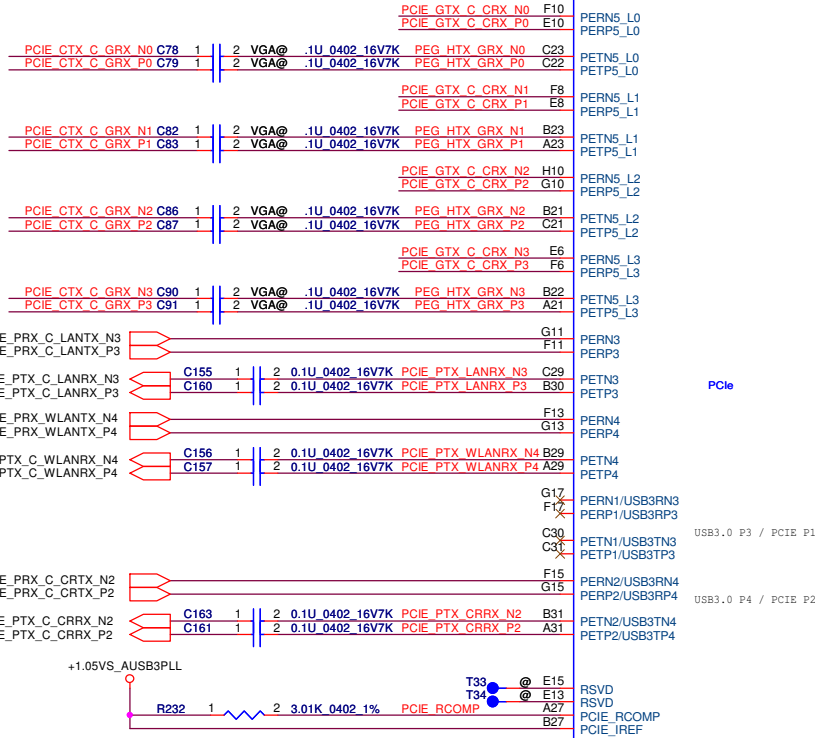




PCIE LAN

WLAN NGFF type

PCIE Card Reader

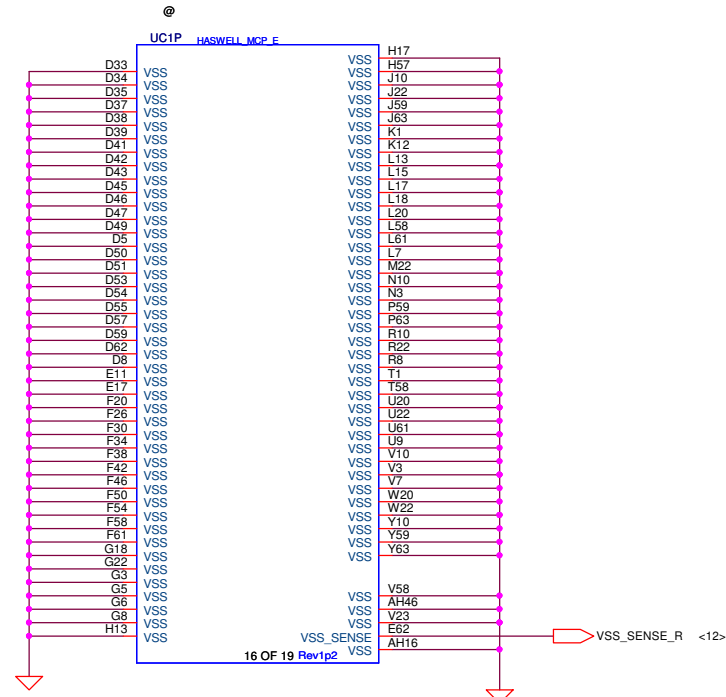
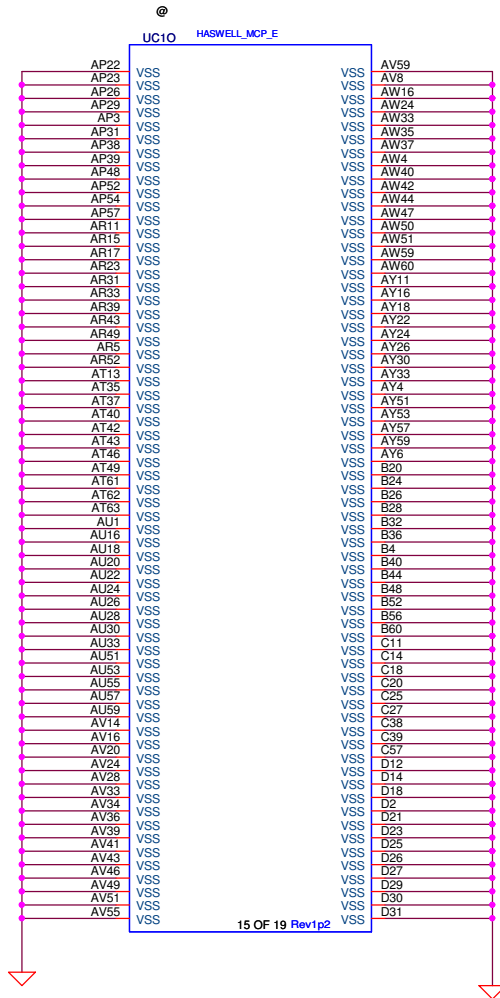
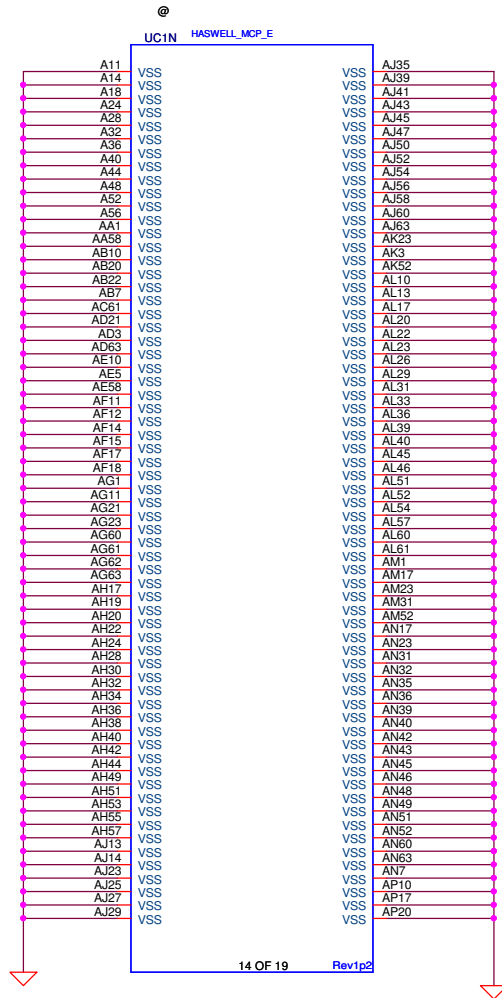


CAD note:  
Route single-end 50-ohms and max 450-mils length.  
Avoid routing next to clock pins or under stitching capacitors.  
Recommended minimum spacing to other signal traces is 15 mils

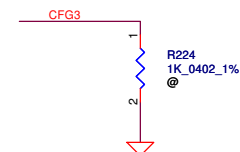
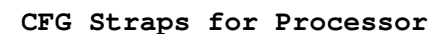
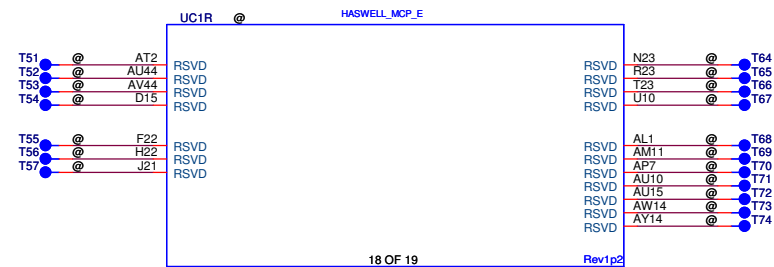
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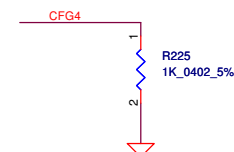




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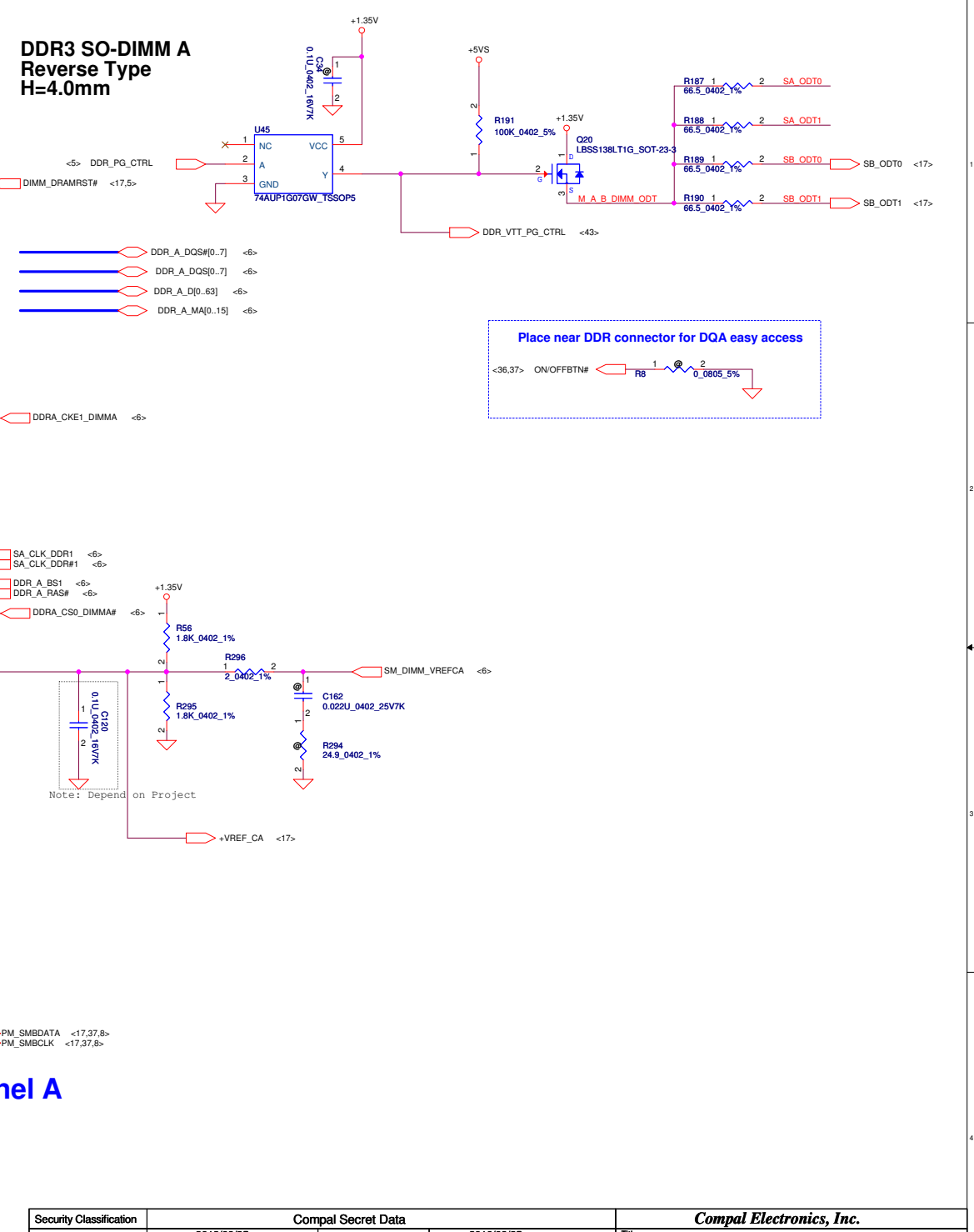
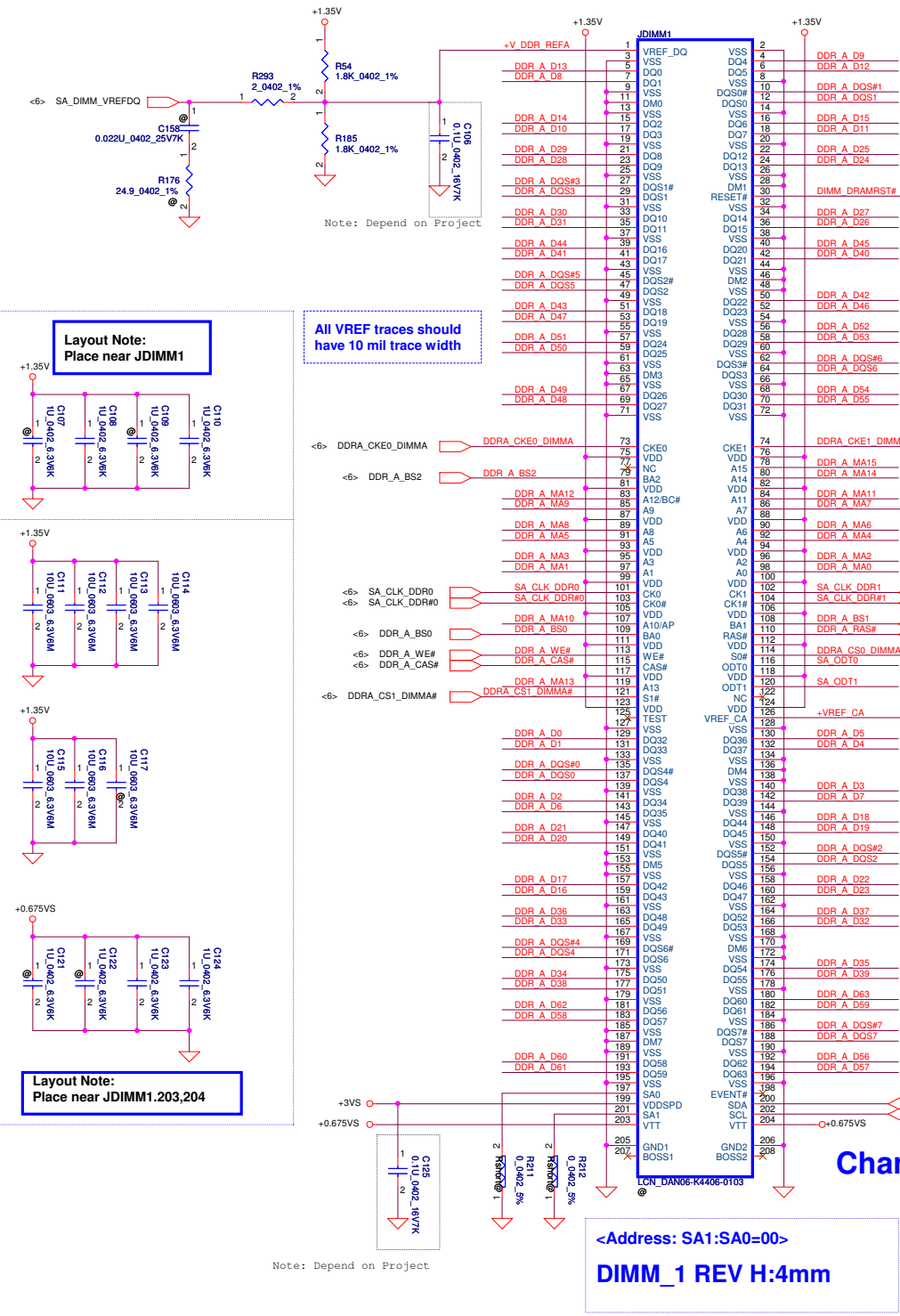


Physical Debug Enable (DFX Privacy)	
CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR



Display Port Presence Strap	
CFG4	<p>1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>





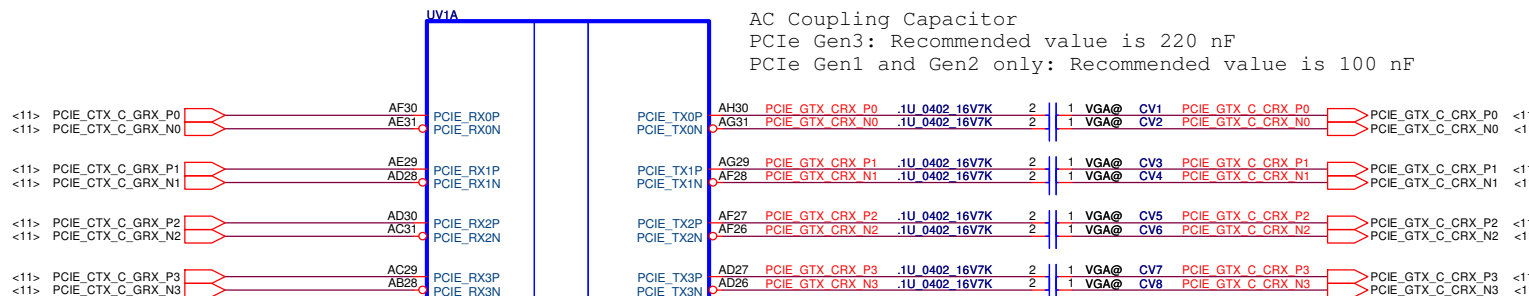
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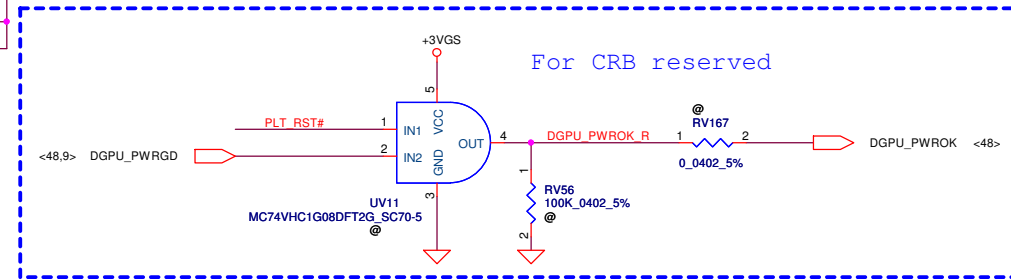
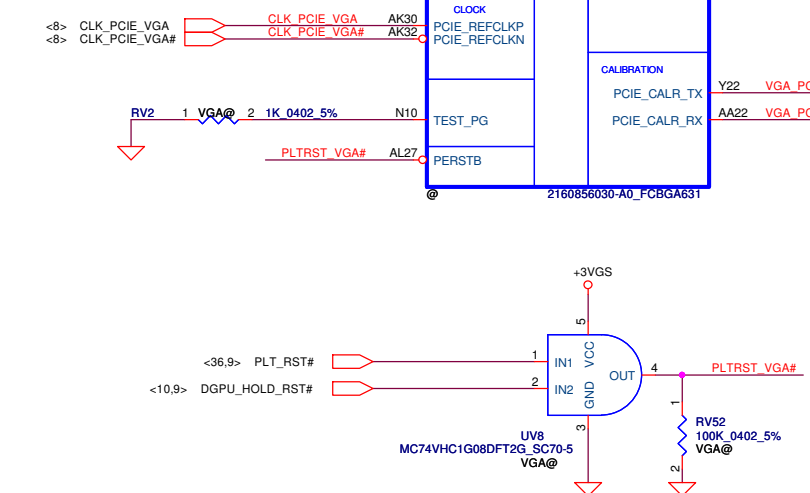
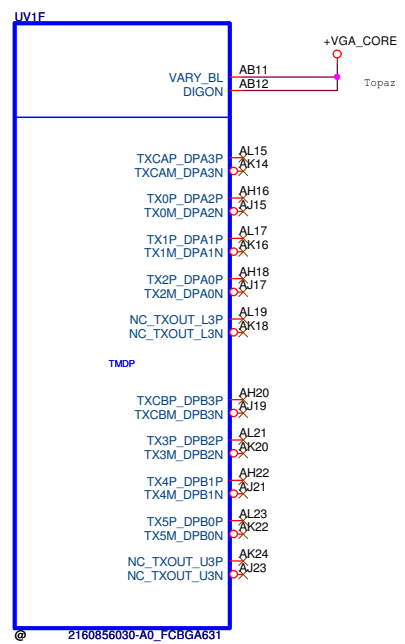


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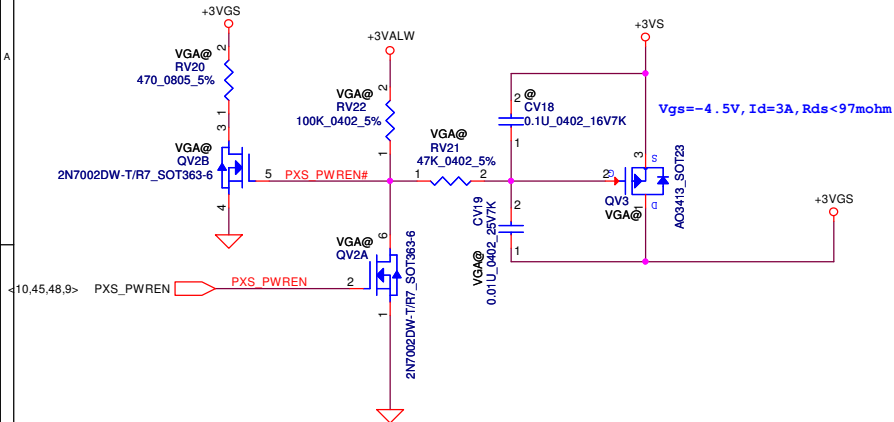
LVDS Interface



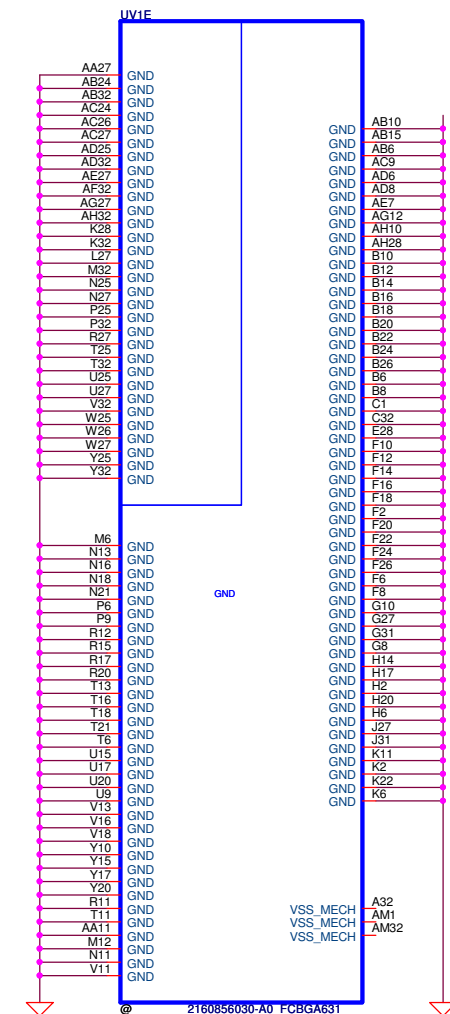
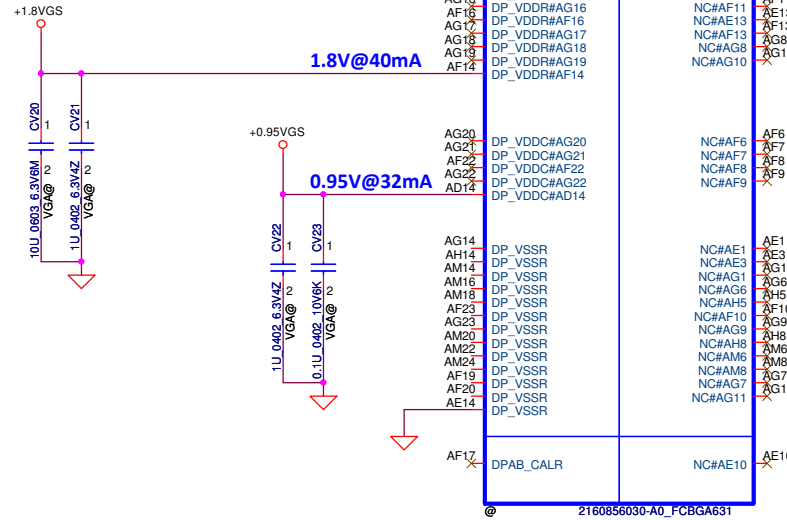
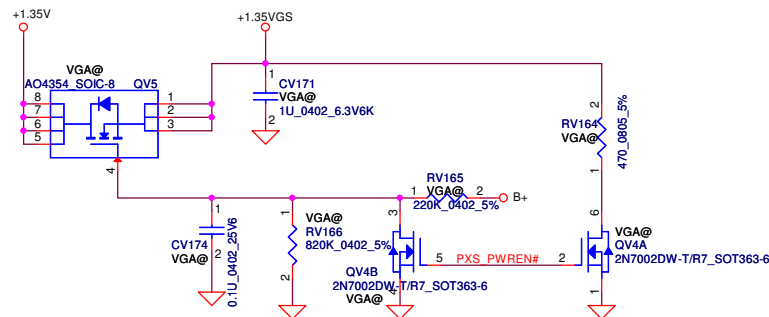
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### +3VS to +3VGS (25mA)



### +1.35V to +1.35VGS (6.5A)



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VDDR1	Jet	CRB	Design
0.01u	1	1	1
0.1u	1	1	1
2.2u	5	5	5
10u	1	1	1

VDD_CT	Jet	CRB	Design
1u	1	1	1

VDDR3	Jet	CRB	Design
1u	1	1	1

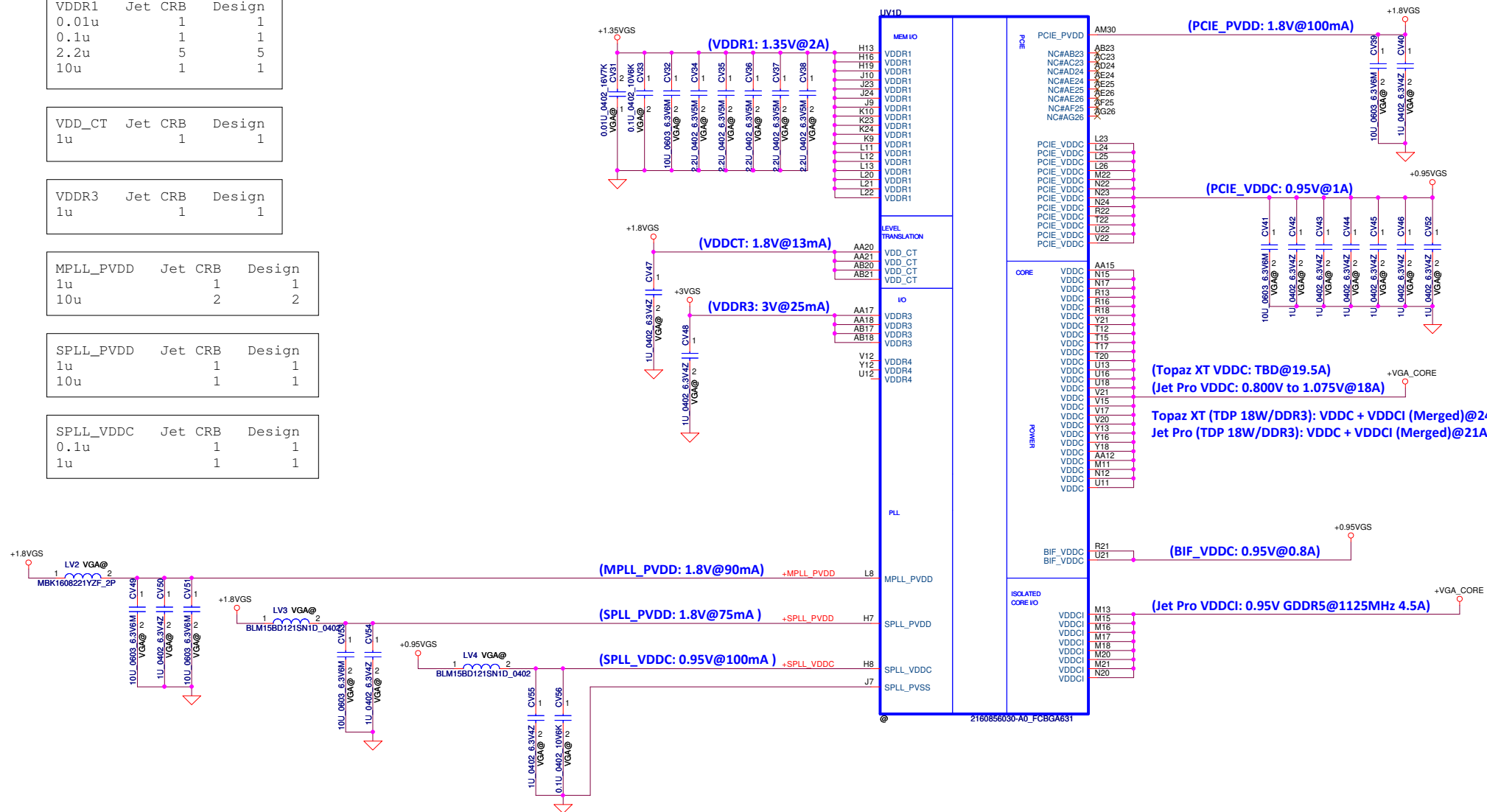
MPLL_PVDD	Jet	CRB	Design
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10u	2	2	2

SPLL_PVDD	Jet	CRB	Design
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10u	1	1	1

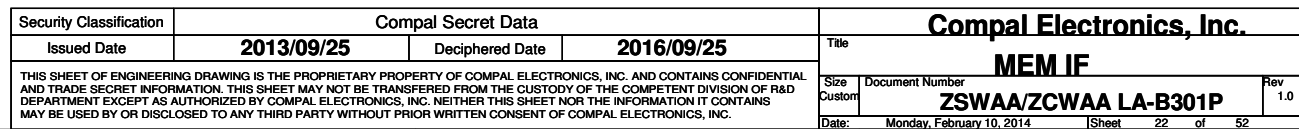
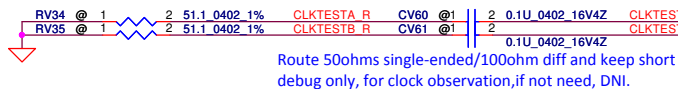
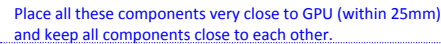
SPLL_VDDC	Jet	CRB	Design
0.1u	1	1	1
1u	1	1	1

PCIE_PVDD	Jet	CRB	Design
1u	1	1	1
10u	1	1	1

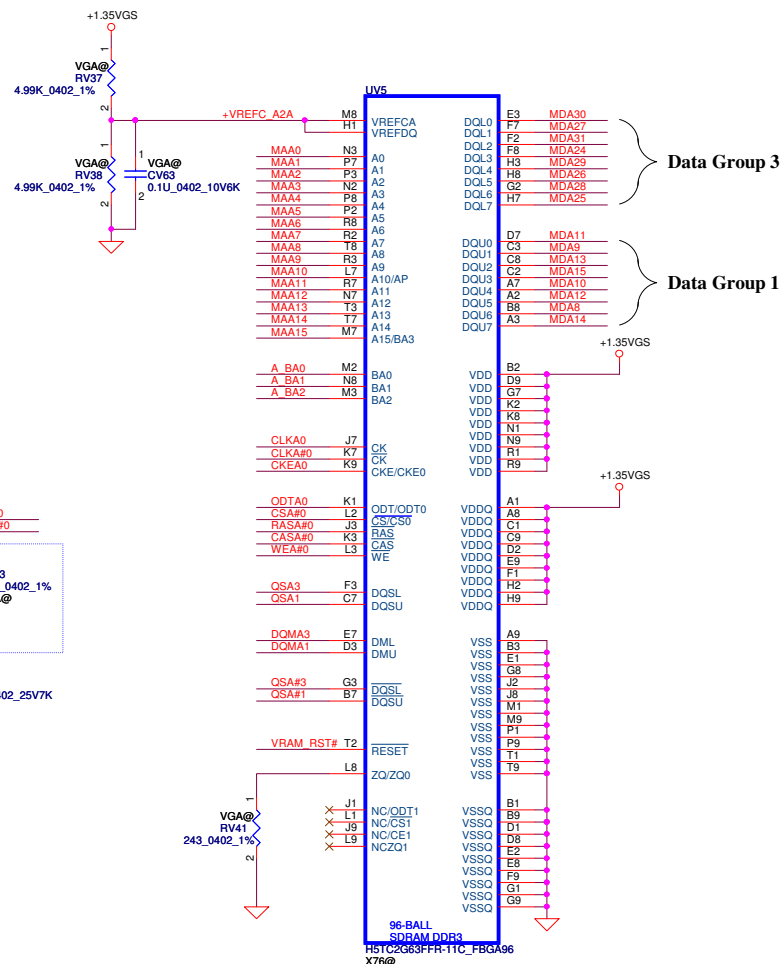
PCIE_VDDC/BIF_VDDC	Jet	CRB	Design
1u	6	6	6
10u	1	1	1



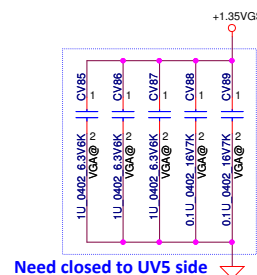
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				Custom	ZSWAA/ZCWAA LA-B301P	1.0
				Date:	Monday, February 10, 2014	Sheet 21 of 52



<Channel A0>



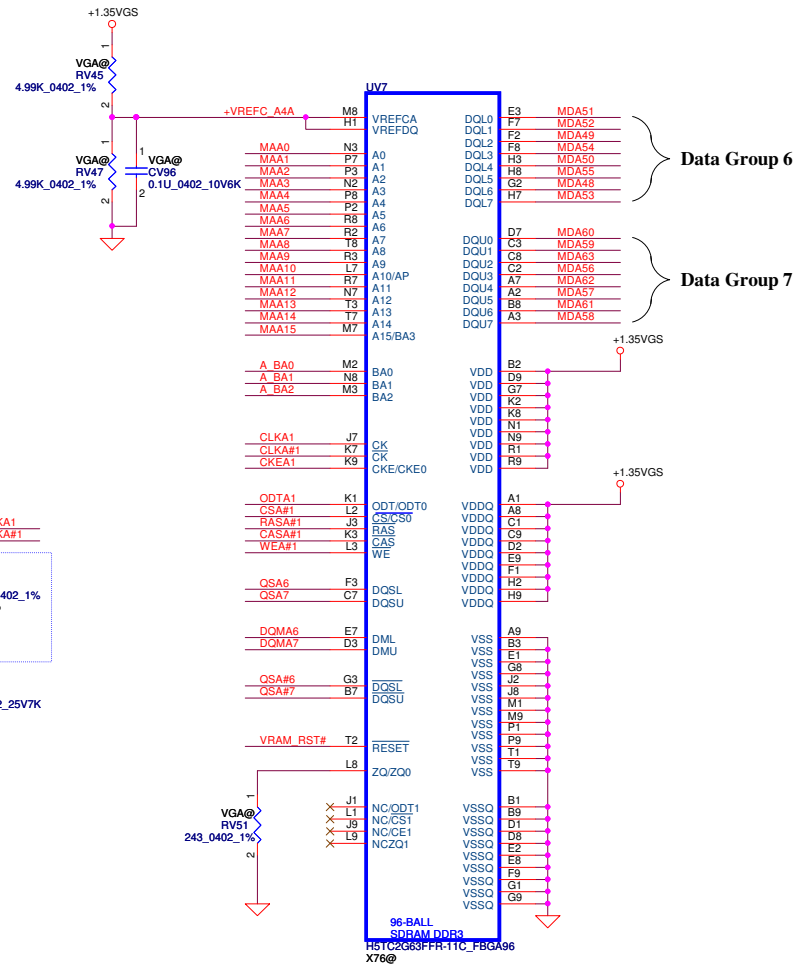
MDA24
MDA25
MDA26
MDA27
MDA28
MDA29
MDA30
MDA31
DQMA3
QSA3
OSA#3



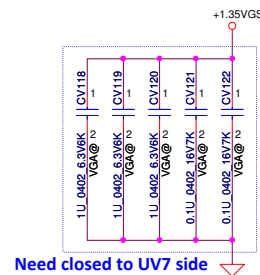
**WWW.AliSaler.Com**



**<Channel A1>**

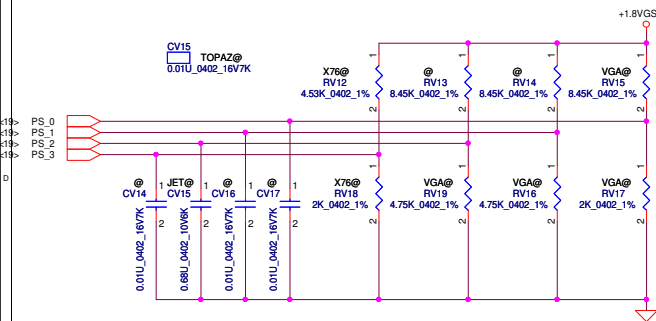


MDA56
MDA57
MDA58
MDA59
MDA60
MDA61
MDA62
MDA63
DQMA7
QSA7
QSA#7





Pin Name	Type	PD/PU	Description
GPIO_0	I/O 3.3 V (VDDR3)	PD-reset	Power-state indicator. Permits the voltage regulator to activate power-saving features. IF VR Support PSI# and DPRSLPVR PU 10K to +3VGS. PSI# :Low load current flag DPRSLPVR : Deeper sleep enable flag
GPIO_5_AC_BATT	I/O 3.3 V (VDDR3)	PD-reset	(Optional) An input which allows the system to request a fastpower reduction by setting GPIO_5_AC_BATT to low (0 V). The resulting state transition may disturb the display momentarily. Power reductions that are less time critical should use the standard software methods in order to prevent display disturbances.
GPIO_6 GPIO_15_PWRCNTL_0 GPIO_20_PWRCNTL_1 GPIO_29 GPIO_30	I/O 3.3 V (VDDR3)	PD-reset	Voltage control signals for the core (VDDC and VDDCI). At reset, these signals will be inputs with weak internal pulldown resistors. The VBIOS can define all voltage-control signals to be either 3.3-V or open-drain outputs (all signals must be the same type). The output states (high/low) of these pins are programmable for each AMD PowerPlay state when they are used as voltage control signals. Note: GPIO_29 and GPIO_30 are only available on 28-nm ASICs, and are NC on earlier generation ASICs.
GPIO_8_ROMSO	I 3.3 V (VDDR3)	PD-reset	Serial-ROM output from ROM. General purpose I/O or open-drain output. <b>Design: No use external VGA ROM, so use the test point</b>
GPIO_9_ROMSI	O 3.3 V (VDDR3)	PD-reset	Serial-ROM input to ROM. General purpose I/O or open-drain output.
GPIO_10_ROMSCK			Serial-ROM clock to ROM. General purpose I/O or open-drain output.
GPIO_22_ROMCSB			BIOS-ROM chip select. Used to enable the ROM for ROM read and program operations. <b>Design: No use external VGA ROM, so use the test points.</b>
GPIO_17_THERMAL_INT	I/O 3.3 V (VDDR3)	PD-reset	Thermal monitor interrupt. An input from an external temperature sensor (ALERTb).
GPIO_19_CTF	O 3.3 V (VDDR3)	PD-reset	Critical temperature fault (CTF) (active high) will output 3.3 V if the on-die temperature sensor exceeds a critical temperature so that the motherboard can protect the ASIC from damage by removing power. The CTF setpoint is 109°C by default, and is programmed during ASIC initialization. See the advisory for AMD PowerPlay states for more details.
GPIO_21	I/O 3.3 V (VDDR3)	PD-reset	(Optional) Voltage control signal for the memory-voltage regulator. Note: This signal must be low (0 V) at reset (failure to do so will prevent booting).
GPIO_28_FDO	I/O 3.3 V (VDDR3)	PD-reset	Disable MLPS: PU 10K ohm to 3.3V. (Do not install for Mars) Enable MLPS: PD 10K ohm to GND. (Install for Mars)
CLKREQB	O		Supports the CLKREQB feature for saving power to turn on/off the REFCLK clock on the ASIC.
PX_EN	O	PD	On/off regulator switch in AMD PowerXpress? (switchable graphics) BACO mode. High (3.3 V) switches the regulators off (enter BACO mode). Low (0 V) switches the regulators on. (Default) PX_EN is tri-state before internal TEST_PG is asserted and PERSTb is deasserted.



PS\_3[3:1]

Memory ID	P/N	Vendor	Configuration	Size
000	SA000068U40	Samsung	K4W2G1646Q-BC1A	1G
001	SA00006H400	Hynix	H5TC2G63FFR-11C	1G
010	SA00005XB00	Micon	MT41K128M16JT-107G:K	1G
011	SA000076P00	Samsung	K4W4G1646D-BC1A	2G
100	SA00006E800	Hynix	H5TC4G63AFR-11C	2G
101	SA000065D00	Micon	MT41K256M16HA-107G:E	2G

## MLPS

MLPS Bit	Strap Name	Legacy	Description	Settings
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	GPIO[13:11]	If BIOS_ROM_EN = 1, ROM_CONFIG[2:0] define the ROM type. If BIOS_ROM_EN = 0, ROM_CONFIG[2:0] define the primary memory-aperture size. Refer to current databooks for details.	001
PS_0[4]	N/A	GENLK_VSYNC	Reserved for internal use only. Must be 1 at reset.	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	GPIO_2	Re-defined strap to indicate PCIe GEN3 capability. 1 = PCIe GEN3 supported. 0 = PCIe GEN3 not supported.	0
PS_1[2]	STRAP_BIF_CLK_PM_EN	GPIO_8	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	GENLK_CLK	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	TX_PWRS_ENB	GPIO_0	Transmitter (Tx) power savings enable. 0 = 50% Tx output swing. 1 = Full Tx output swing.	1
PS_1[5]	TX_DEEMPH_EN	GPIO_1	PCI EXPRESS transmitter, deemphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	1
PS_2[1]	N/A	N/A	Reserved.	0
PS_2[2]	N/A	N/A	Reserved.	0
PS_2[3]	BIOS_ROM_EN	GPIO_22	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	0
PS_2[4]	BIF_VGA_DIS	GPIO_9	VGA disable determines whether or not the card will be recognized as the system's VGA controller. 0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.	0
PS_2[5]	N/A	N/A	Reserved.	0
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	N/A	Board configuration related strapping (such as memory ID).	Base on VRAM ID
PS_0[5] PS_3[4] PS_3[5]	AUD_PORT_CONN_PINSTRAP[0] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[2]	N/A	Together with PS_0[5] form the three-bit strap option to indicate the number of audio-capable display outputs. In a given ASIC there are as many endpoints as there are digital display outputs, though not all outputs are audio capable. 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	111

## MLPS Strap

	Bits[5:4]	Bits[3:1]	Capacitor	R_pu	R_pd
PS_0[5:1]	11	001	NC	8.45K	2K
PS_1[5:1]	11	000	NC	NC	4.75K
PS_2[5:1]	00	000	680 nF	NC	4.75K
PS_3[5:1]	11	XXX	NC	X	X

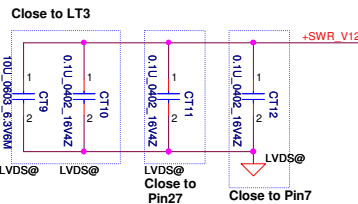
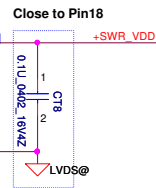
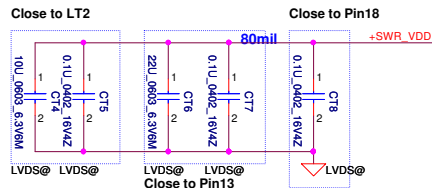
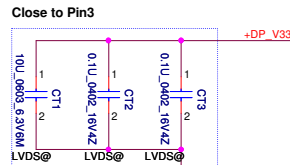
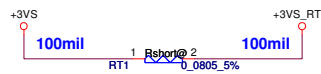
00 for JET  
10 for Topaz

Mapping to VRAM type

## Primary Memory Aperture Size Requested at PCI Configuration

Size of the Primary Memory Apertures	ROM_CONFIG [2:0]	MLPS configuration
		Bits[5:1] PU(1%) PD(1%) Cap
128 MB	000	xx000 NC 4.75k
256 MB	001	xx001 8.45k 2.00k
64 MB	010	xx010 4.53k 2.00k
Reserved	011	xx011 6.98k 4.99k
512 MB	Not supported	xx100 4.53k 4.99k
1 GB	Not supported	xx101 3.24k 5.62k
2 GB	Not supported	xx110 3.40k 10.0k
4 GB	Not supported	xx111 4.75k NC
		00xxx 680nF
		01xxx 82nF
		10xxx 10nF
		11xxx NC

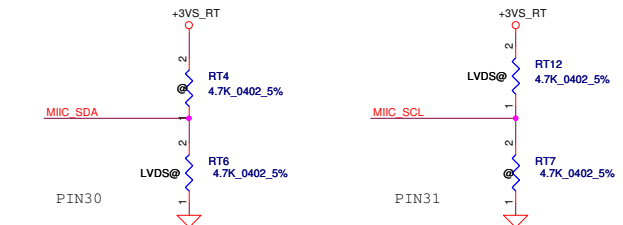
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## Mode Configure

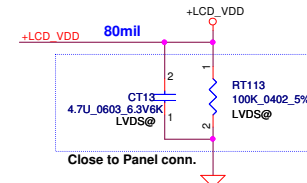
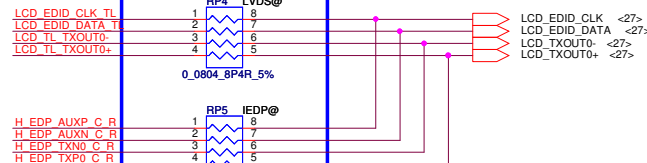
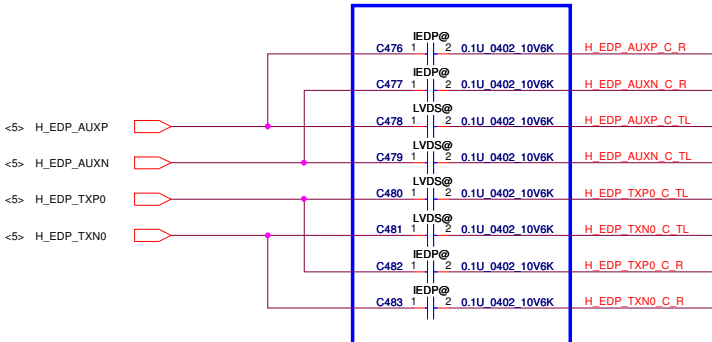
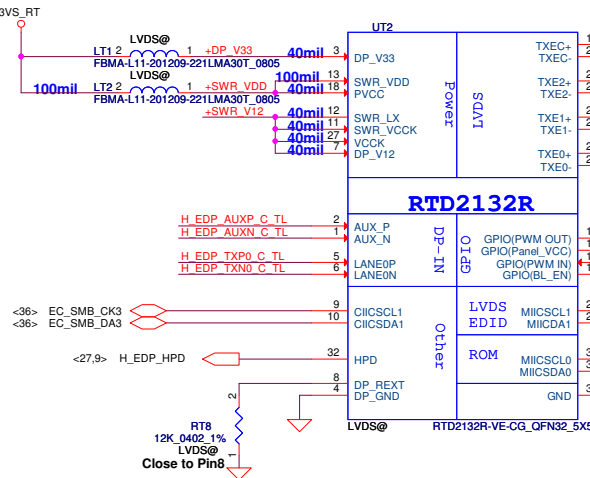
※ROM only mode : PIN 30 4.7k pull low, Pin 31 4.7k pull high.  
EP mode : PIN 30 4.7k pull high, Pin 31 4.7k pull low.  
EEPROM : PIN 30 4.7k pull high, Pin 31 4.7k pull high.

< ※Default mode >

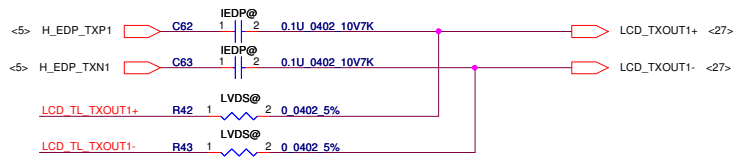


## SWR / LDO Mode select

※LDO mode is adopted as default power regulator mode.  
Also can implement SWR mode by add inductor.



Place co-layer Resistor back to back on TOP and BOT



	PIN15
2132S	TL_ENVDD
2132R	+LCD_VDD *

\* Version R internal Power Switch, can output 1A, Rds(on)=0.2 ohm

PIN16	Accept voltage input (high level)
2132S	3.3V
2132R	1.5~3.3V

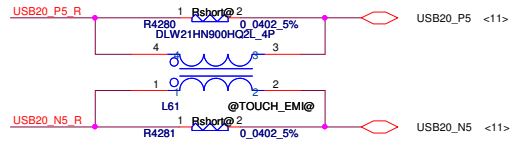
\* Version R has internal level shifter, remove level shifter circuit on AMD platform

## Different between 2132S and 2132R(N)

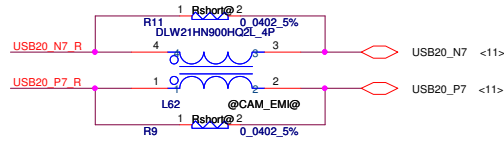
2132S	2132R(N)
1. Support SWR mode	1. Support LDO mode and SWR mode 2. Internal ROM 3. Support LCD_VDD(internal Power switch) 4. Integrates Level shifter

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BTO : TOUCH\_EMI@



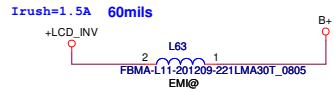
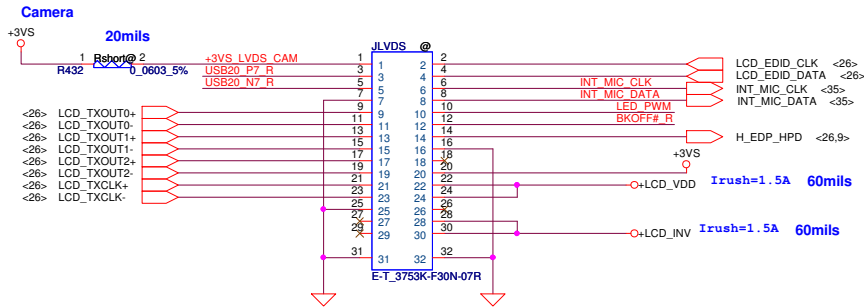
EMI request - Close to JLVDS connector



Change L62 P/N from SM070003Y00 to SM070003K00

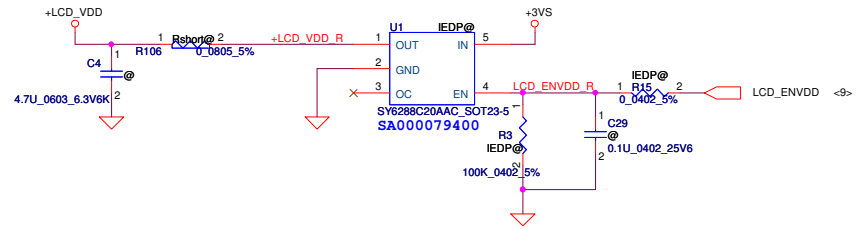
## LVDS colay eDP cable

Pin define will be change after ME ready

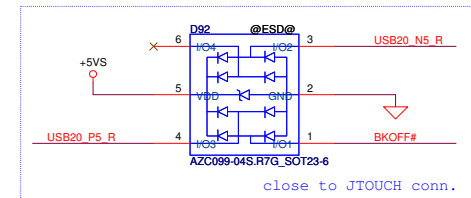
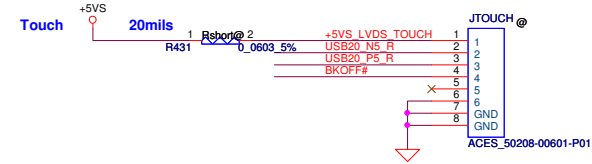
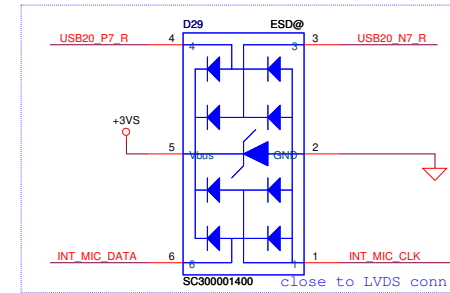


## LCD POWER CIRCUIT (For EDP panel only)

I rush=2A  
W=80mils



## Camera & MIC



Change D15,D90,D91 P/N from SCS0340L010 to SCS00003500 for X code.

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HDMI TMSD BUS

Colay Cap

Colay Resistor

Choke

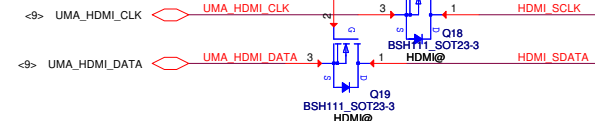
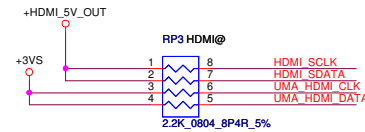
Componet close to Conn.

Impedance depend on platform design guide

HDMI Royalty  
R00000003HM  
HDMI W/Logo + HDCP

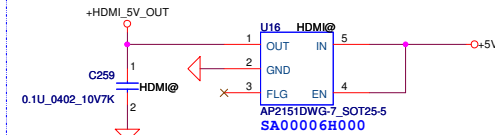
HDMI W/O Logo: R00000001HM  
HDMI W/Logo: R00000002HM  
HDMI W/Logo + HDCP: R00000003HM

please manually load  
this virtual material to 45@ BOM

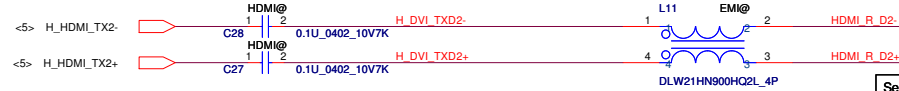
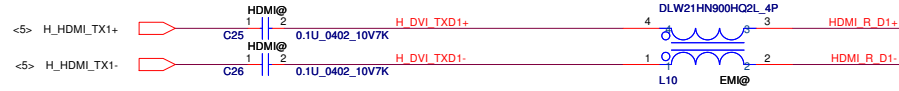
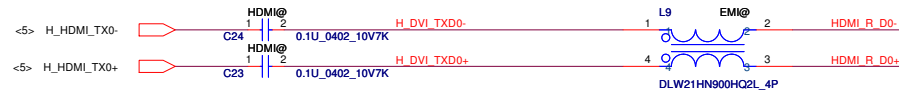
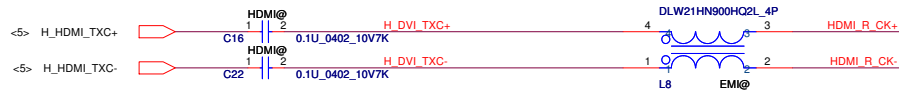


### HDMI POWER CIRCUIT

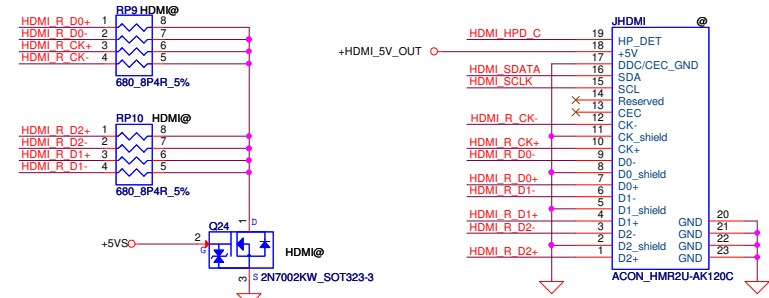
VIN = 5V, IOUT = 0.5A, RDS(ON) TYP=95m ; MAX=115m  
Current Limit: TYP=0.8A ; MAX=1A



Change L8,L9,L10,L11 P/N  
from SM070003Y00 to SM070003K00

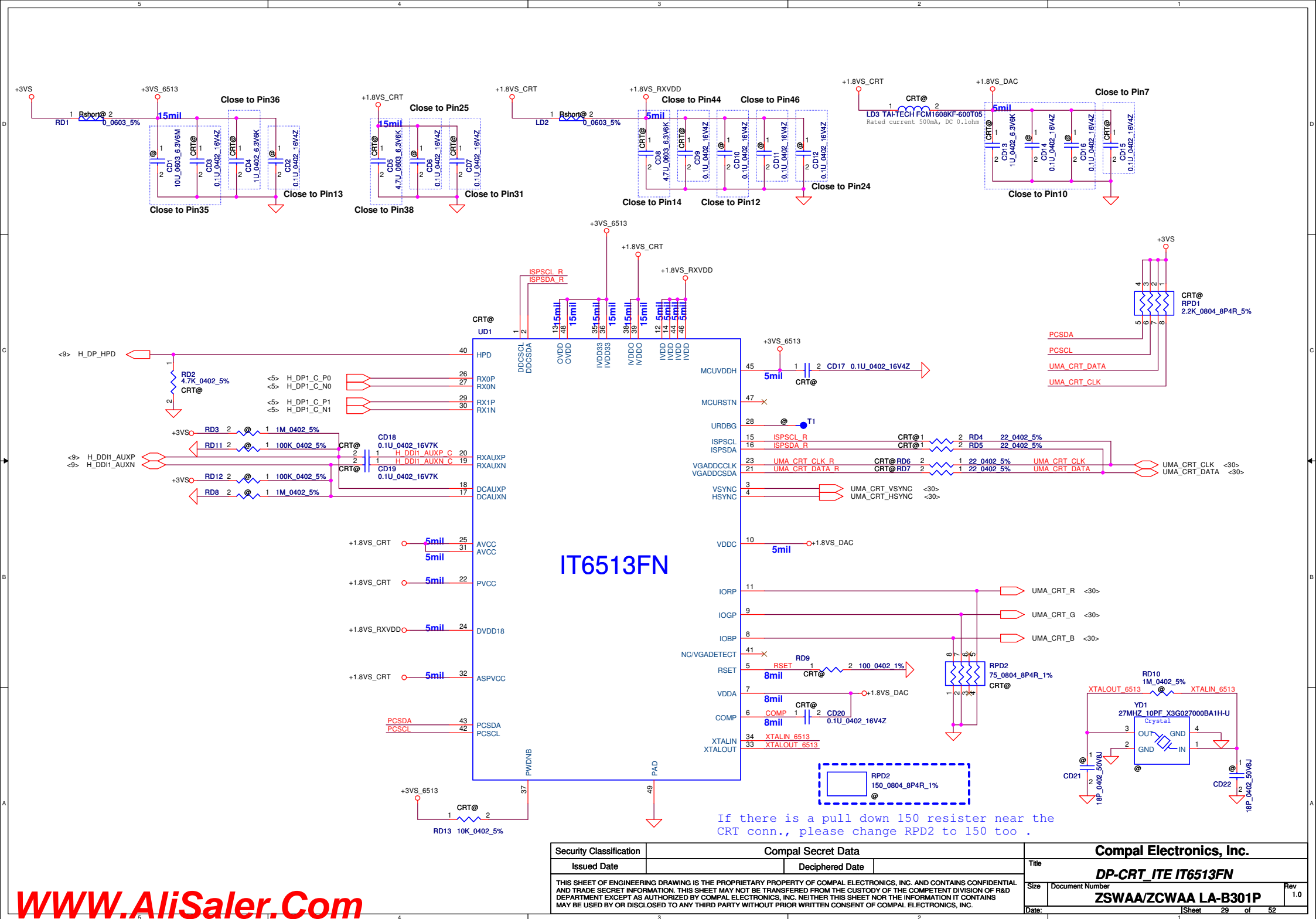


### HDMI Connector



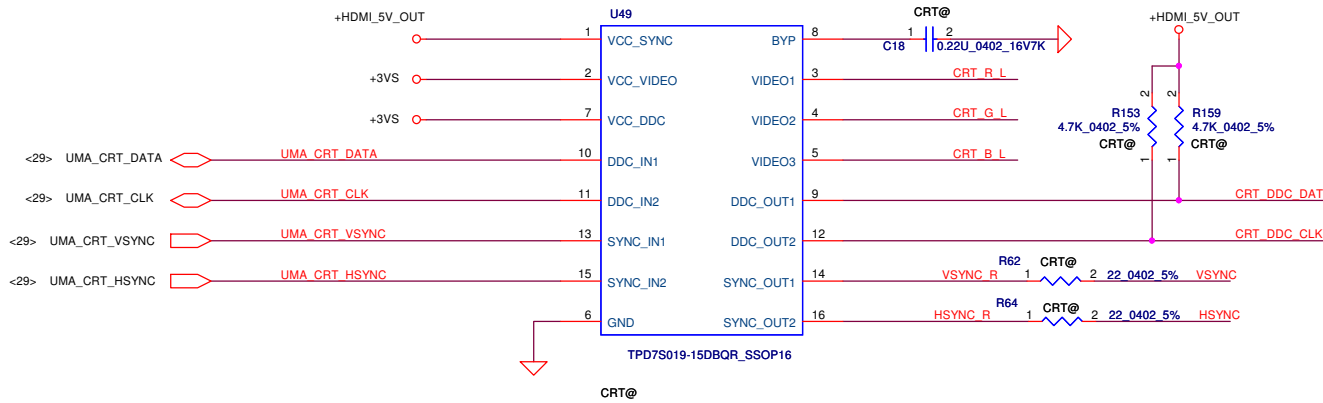
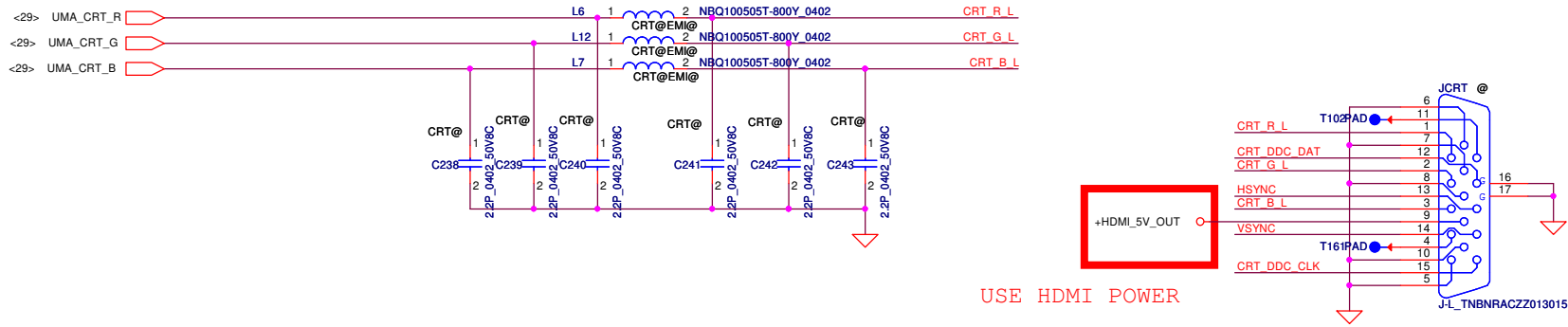
Common CHOKE use 90ohm

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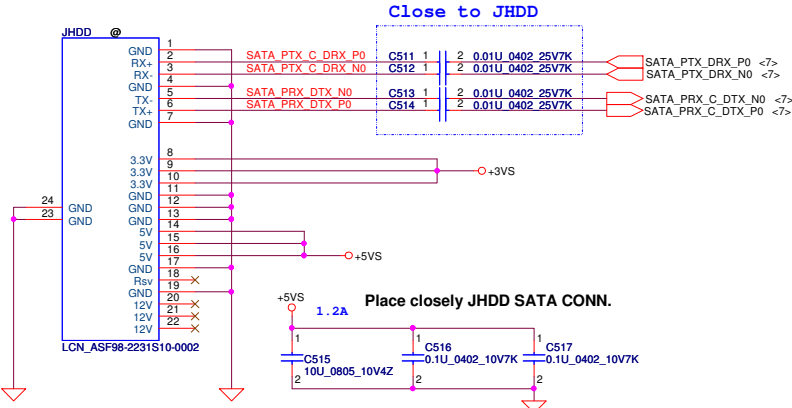
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Date:		Sheet		Rev	
		29		1.0	

# CRT CONNECTOR

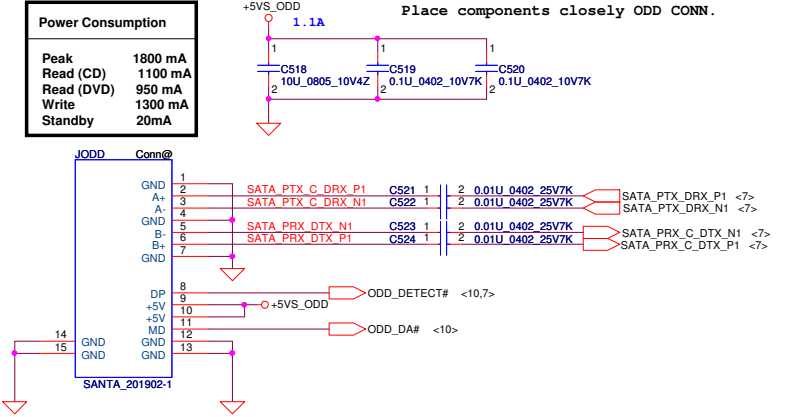


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SATA HDD/SSD Conn.



SATA ODD Conn



# NGFF-Slot1-E-Key-WLAN

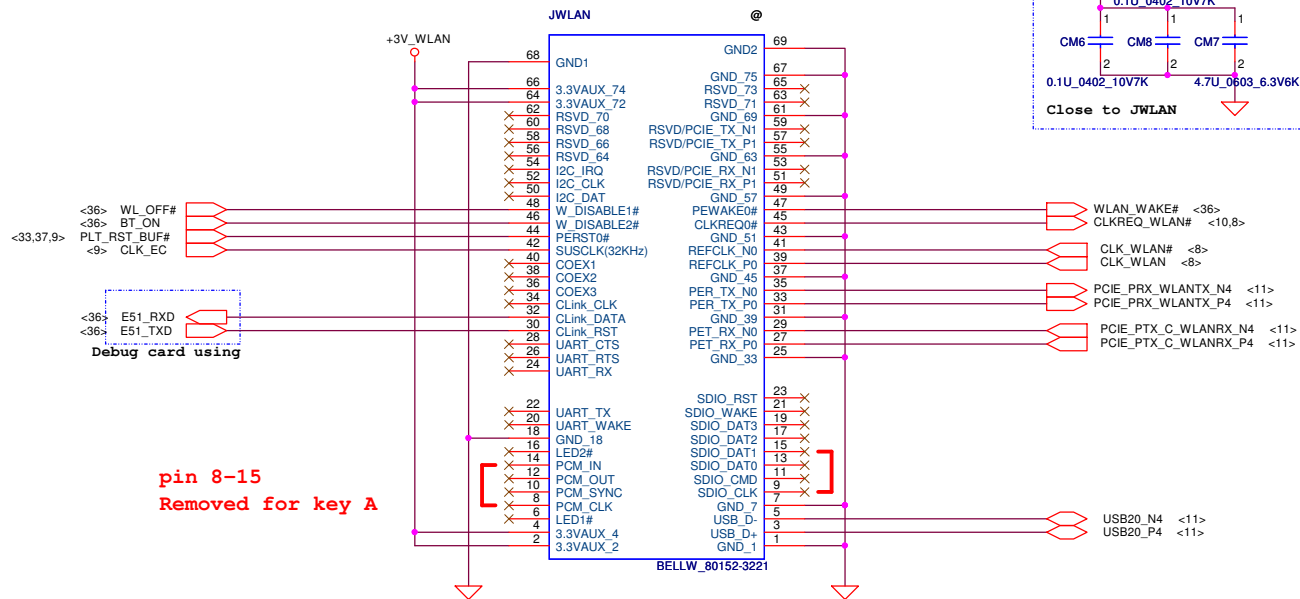


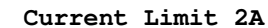
Table 23. SDIO Based Module Solution Pinout (Module Key E)

Pin	Signal	Pin	Signal
74	3.3V	75	GND
72	3.3V	73	RESERVED/REFCLKN1
70	UM_Power_In/GPIO1/PEWake1#	71	RESERVED/REFCLKP1
68	UM_Power_Out/CLKREQ0#	69	GND
66	UM_SWP/PERST#	67	Reserved/PETn1
64	RESERVED	65	Reserved/PCIO1
62	ALERT# (IO/0/3.3)	63	GND
60	I2C CLK (IO/0/3.3)	61	Reserved/PERn1
58	I2C DATA (IO/0/3.3)	59	Reserved/PCIO1
56	W_DISABLE# (IO/0/3.3V)	57	GND
54	Reserved/W_DISABLE#2 (IO/0/3.3V)	55	PEWake# (IO/0/3.3V)
52	PERST# (IO/0/3.3V)	53	CLKREQ# (IO/0/3.3V)
50	SUSCLK12MHz (IO/0/3.3V)	51	GND
48	CORE11V/IO0/L1V	49	REFCLKN0
46	CORE2V/IO0/L1V	47	REFCLKP0
44	CORE3V/IO0/L1V	45	GND
42	VENDOR DEFINED	43	PET#0
40	VENDOR DEFINED	39	GND
38	VENDOR DEFINED	37	PER#0
36	UART_CTS (IO/0/3.3V)	35	PER#0
34	UART_RTS (IO/0/3.3V)	33	GND
32	UART_B# (IO/0/3.3V)	31	GND
30	Module Key	29	Module Key
28	Module Key	27	Module Key
26	Module Key	25	Module Key
24	Module Key	23	Module Key
22	SDIO Reset (IO/0/3.3V)	21	SDIO Wake (IO/0/3.3V)
20	UART Wake (IO/0/3.3V)	19	SDIO DATA0 (IO/0/3.3V)
18	GND	17	SDIO DATA1 (IO/0/3.3V)
16	LED#2 (IO/0/3.3V)	15	SDIO DATA2 (IO/0/3.3V)
14	PCM_IN/US SD_IN (IO/0/3.3V)	13	SDIO DATA3 (IO/0/3.3V)
12	PCM_OUT/US SD_OUT (IO/0/3.3V)	11	SDIO CMD0 (IO/0/3.3V)
10	PCM_SYNC/US WS (IO/0/3.3V)	9	SDIO DATA0 (IO/0/3.3V)
8	PCM_CLK/US SOC (IO/0/3.3V)	7	GND
6	LED#1 (IO/0/3.3V)	5	WAKE_P
4	3.3V	3	WAKE_P
2	GND	1	GND

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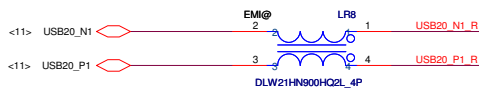
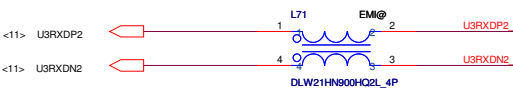
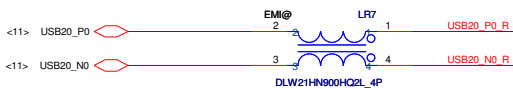
Change LR9 P/N from SM070003Y00 to SM070003K00



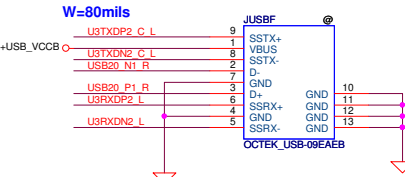
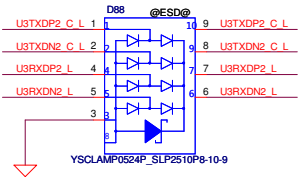
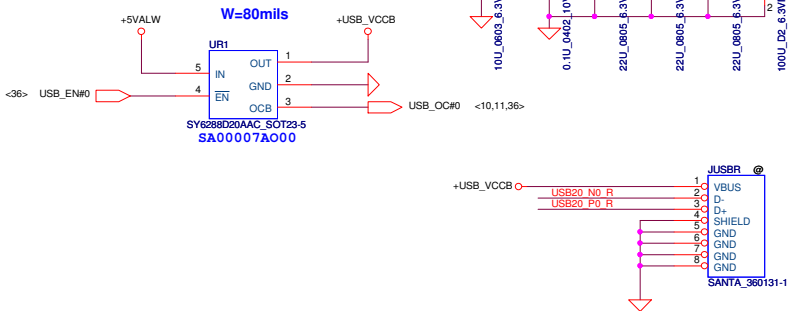
Right rear USB2.0 Conn.

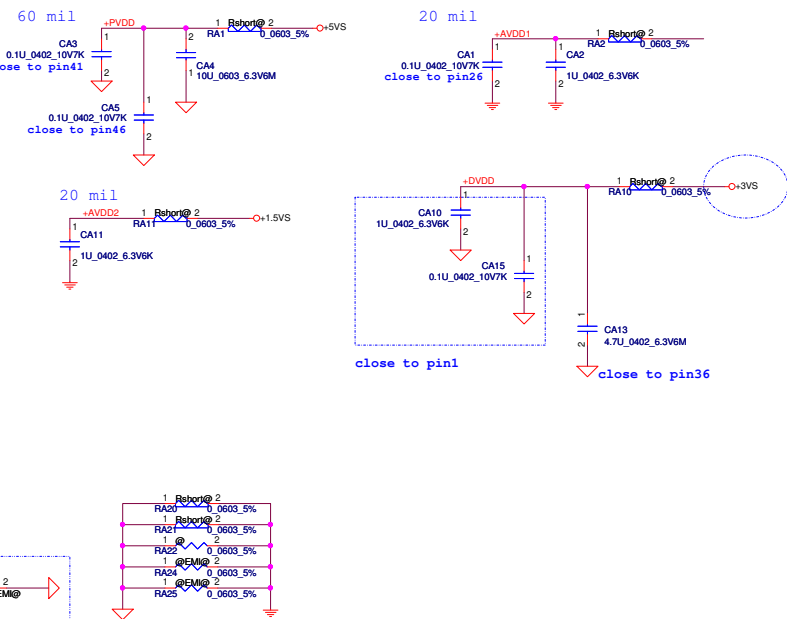
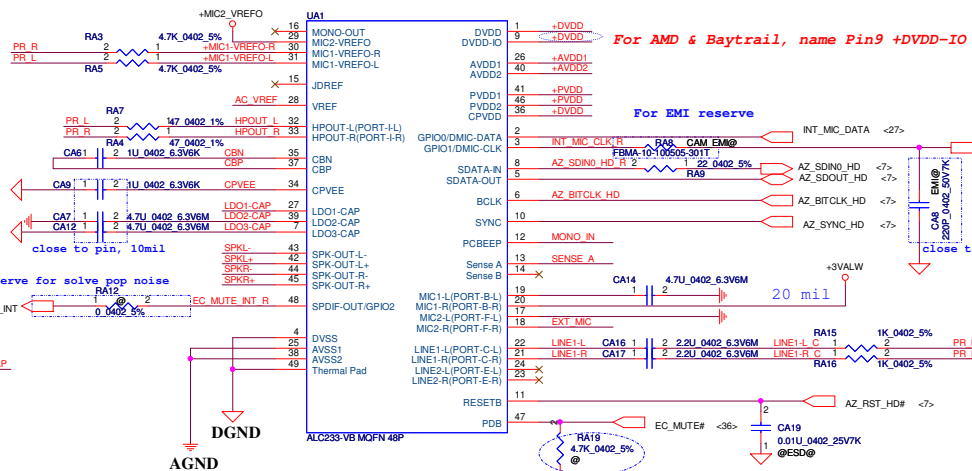
Right side USB 3.0 x 1 W/O Sleep&Charge

Change L71,L72,LR7,LR8 P/N  
from SM070003Y00 to SM070003K00

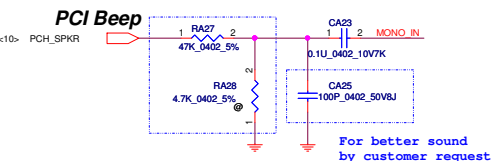


Current Limit 2A



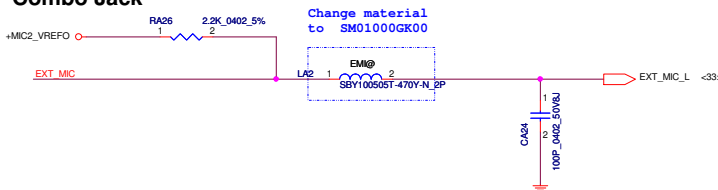


## Beep sound

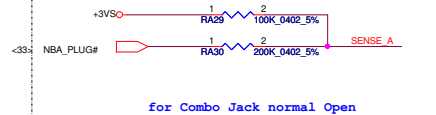


(ALC233 supported iPhone headset/ Headphone/ MIC in)

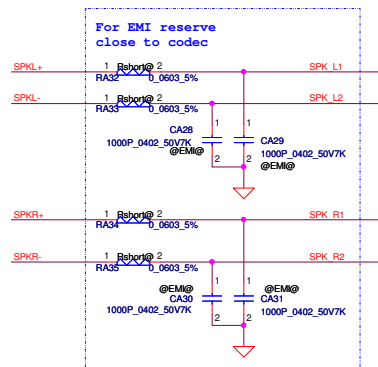
## Combo Jack



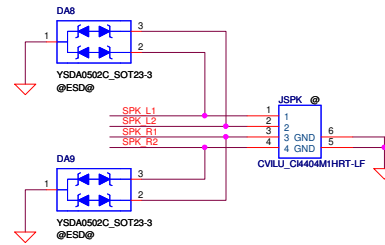
place close to chip



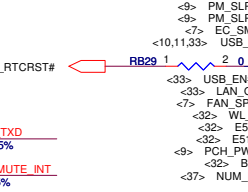
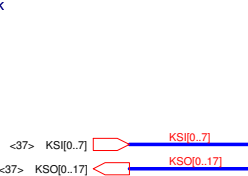
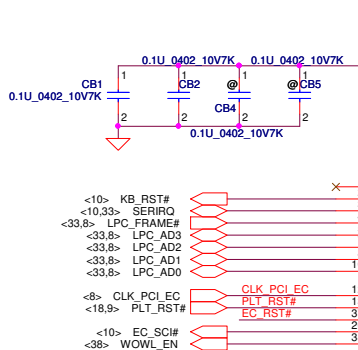
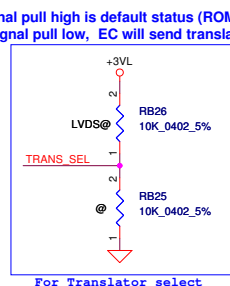
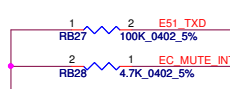
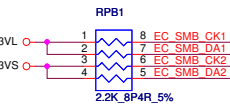
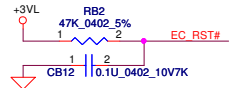
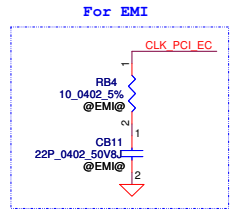
## SPK



## SPK Conn.

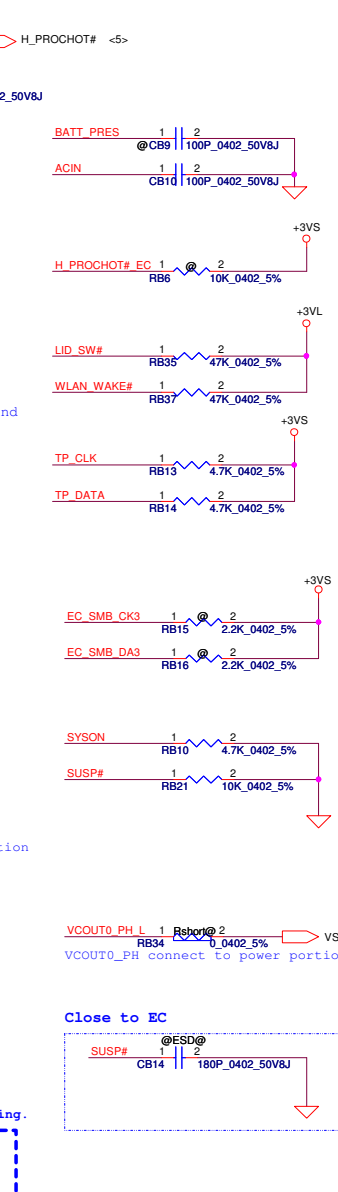
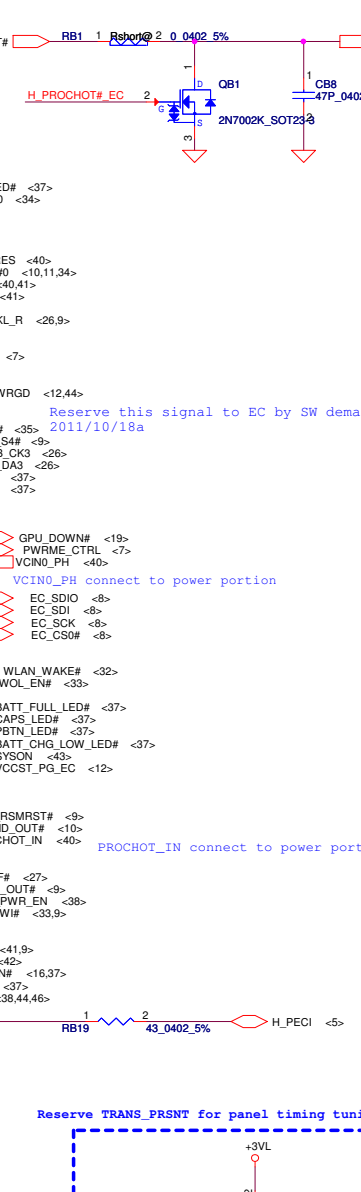
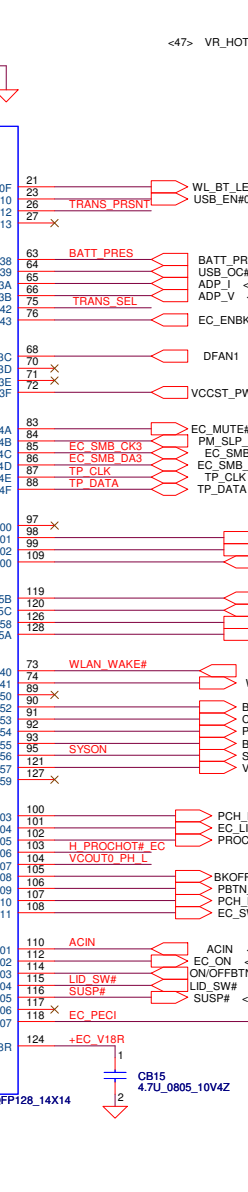
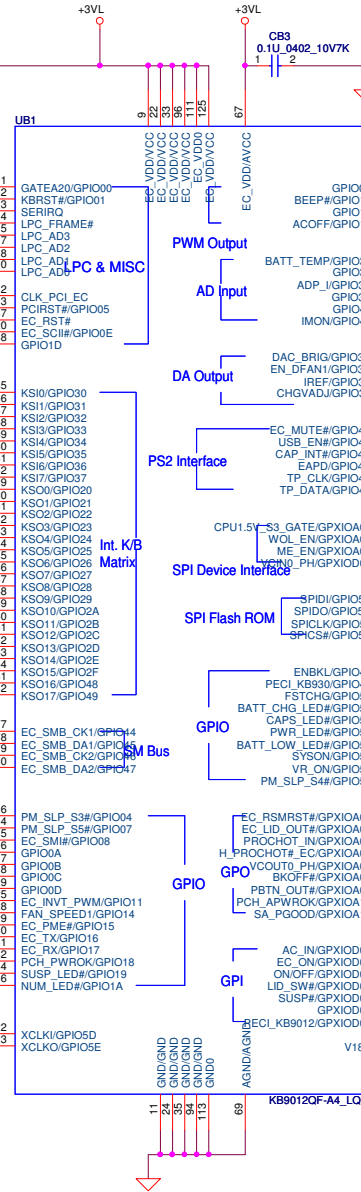


EXT\_MIC · EXT\_MIC\_L · RING2 · RING2\_L  
Speaker 4 ohm: 40mil  
Speaker 8 ohm: 20mil  
RA13 · LA2 · CA24  
close to small board connector



**Voltage Comparator Pins FOR 9012 A3**

VCIN0 pin109	>1.2V	<1.2V
VCIN1 pin102		
VCOUT0 pin104	HIGH (default)	LOW
VCOUT1 pin103	HIGH	LOW (default)



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[illegible]

The diagram shows two separate circuit connections. On the left, a red wire connects the +5VS pin to the top terminal (1) of capacitor C549. The capacitor is labeled '0.1U\_0402\_10V7K' and 'ESD@'. Its bottom terminal (2) is connected to a ground symbol. On the right, a red wire connects the +5VALW pin to the top terminal (1) of capacitor C550. This capacitor is also labeled '0.1U\_0402\_10V7K' and 'ESD@', with its bottom terminal (2) connected to a ground symbol.

Need mount RM3 if system don't support ZP0DD

Part number is SA000070S00  
VIN 0.8V-5.5V (VBIAS=5V), IMAX=4A, Rds=22mohm

U7 ZP0DD@  
VIN VIN  
VOUT VOUT  
ON ON  
CT CT  
VBIAS VBIAS  
GND GND

YPS22067DSGR\_SON8\_2X2

U7 ZP0DD@  
C543 10µF 6.3V  
C544 10µF 10V  
ZP0DD@ 270pF 50V7K

please refer to the table to choose C545

**+3VALW TO +3V\_WLAN**

for WOWL

Need mount RM5 if system don't support ISCT

Part number is SA000070S00  
VIN 0.8V~5.5V (VBIAS=5V), IMAX=4A, Rds=22mohm

TPS22967DSGR\_SONB\_2X2

ISCT@

VIN VIN VOUT VOUT ON CT VBIAS GND GND

+3VALW

C546 1U\_0402\_6.3VK

WOWL\_EN

WOWL\_EN

+5VALW

+3V WLAN LS

ISCT@

RM7 0\_0805\_5%

+3V WLAN

C547 0.1U\_0402\_10VK

ISCT@

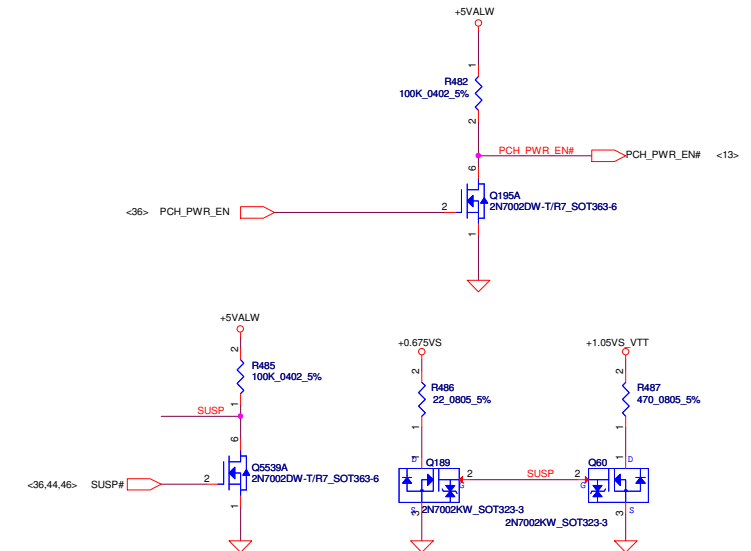
C548 270P\_0402\_50VK

please refer to the table to choose C548

RM4 10K\_0402\_5% NOISCT@

WOWL\_EN

RM2 10K\_0402\_5% ISCT@

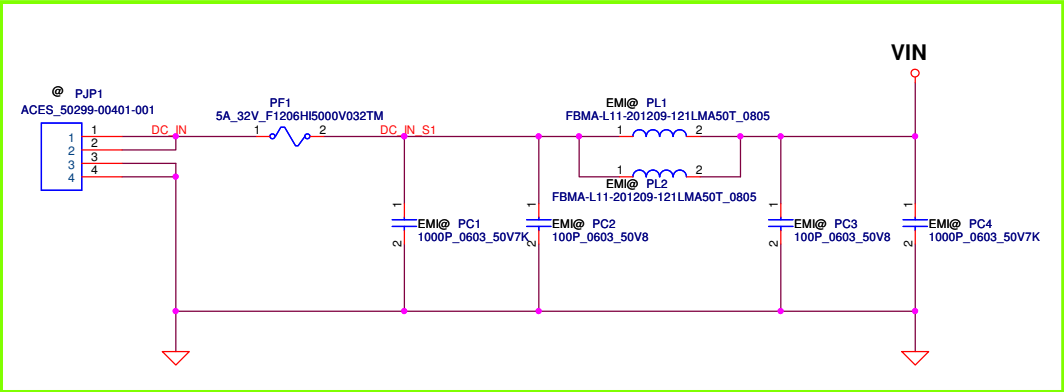


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Mark Green frame that means this part is not belong to layout module part .

Function Field :

Support 37.1  
RTC 38.2  
EMI Part 47.1

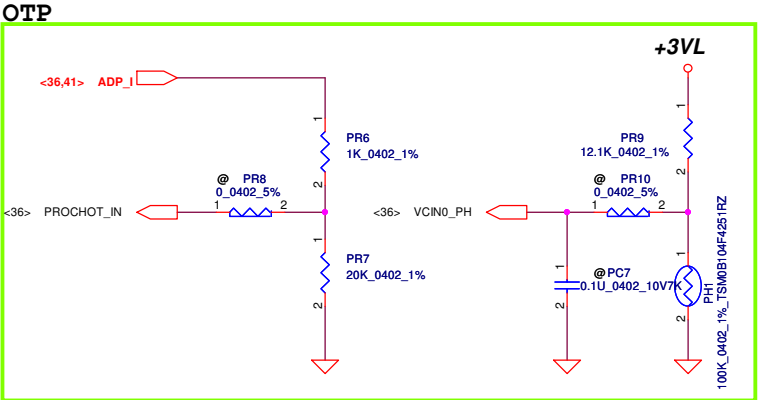
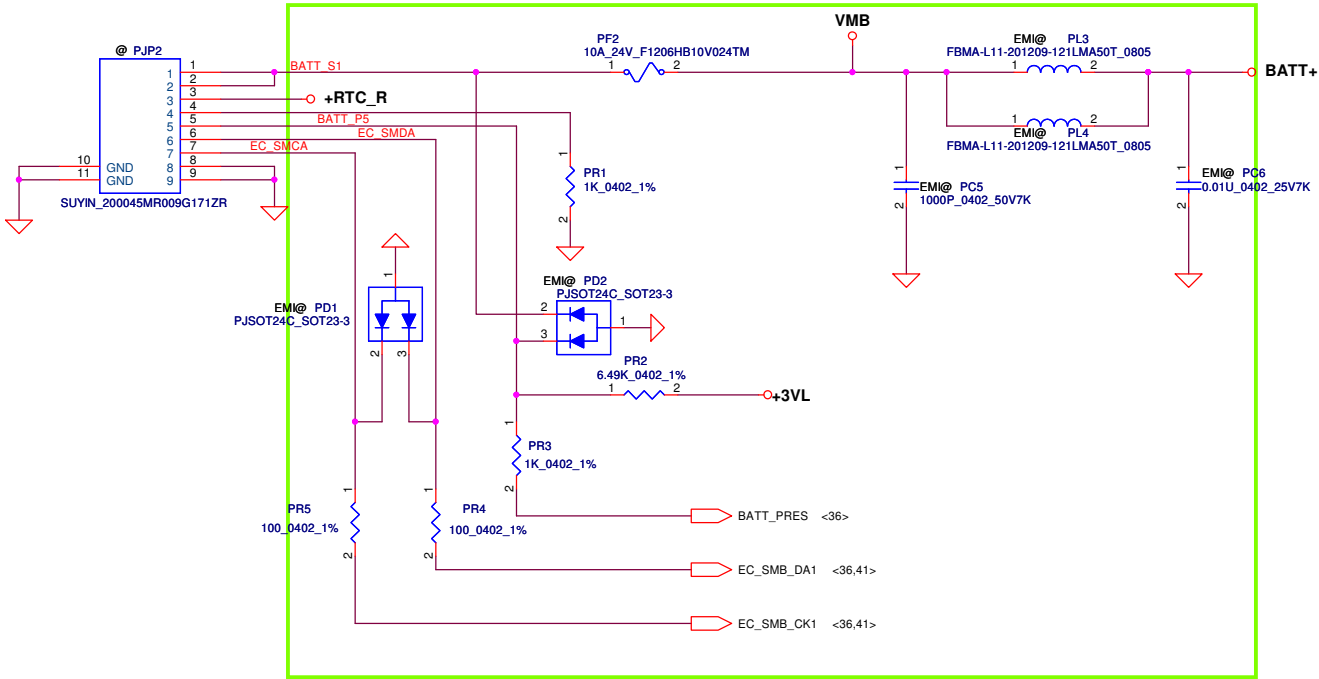


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Size	Document Number			Rev	
A3	ZSWAAZCWAA LA-B301P			1.0	
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Mark Green frame that means this part is not belong to layout module part .

Function Field :

Support 37.1  
OTP 39.7  
EMI Part 47.1  
ESD DIODE 47.2



	Initial	Recovery
45W UMA	0.55V	0.43V

	Initial	Recovery
CPU OTP	90 C	70 C

Security Classification	Compal Secret Data				Compal Electronics, Inc.		
Issued Date	2011/06/15	Deciphered Date	2012/07/11		Title	Battery Conn / OTP	
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# Module model information

BQ24735A\_V1.mdd

BQ24735A\_V2.mdd

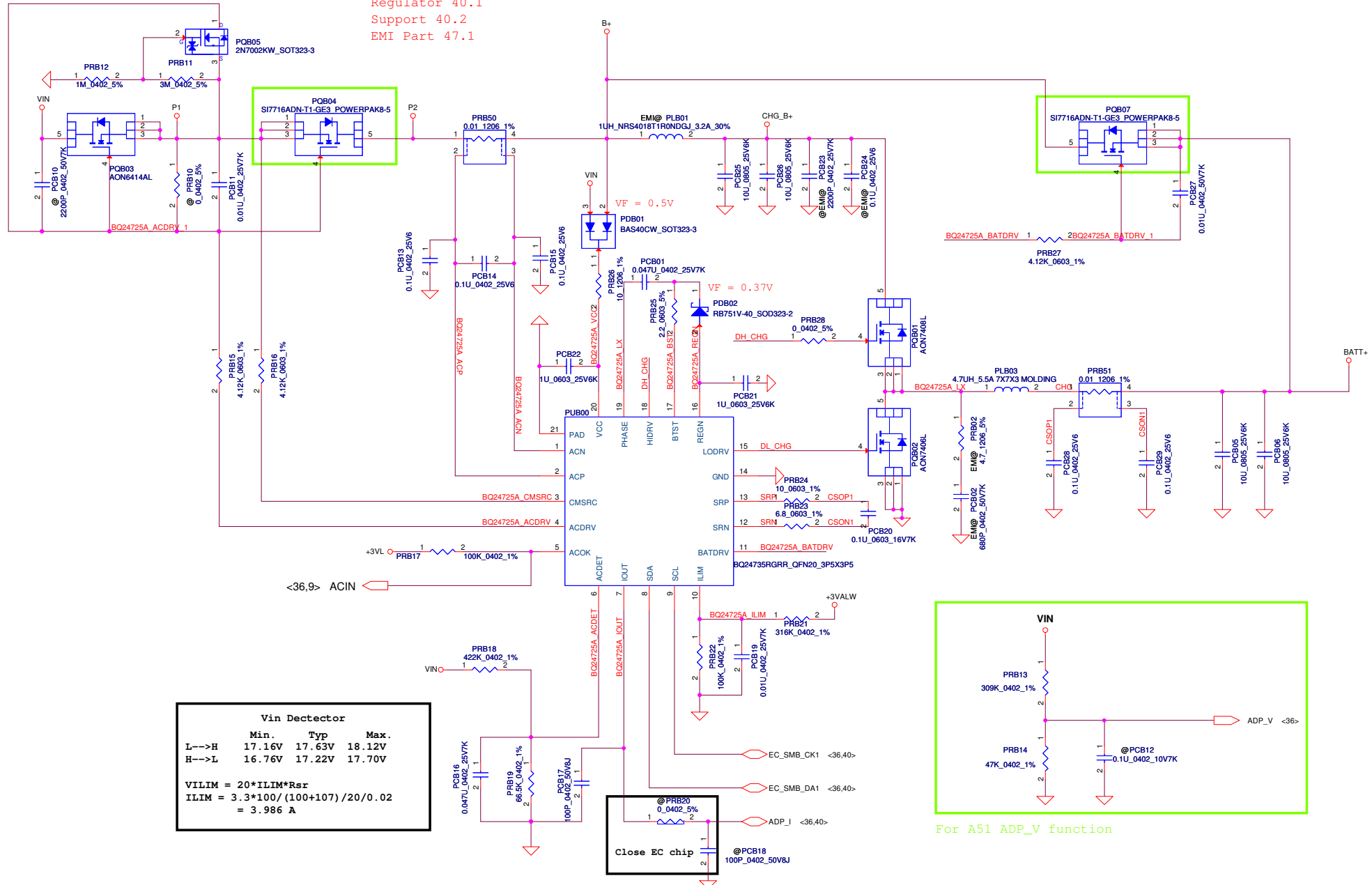
Mark Green frame that means this part is not belong to layout module part .

## Function Field :

Regulator 40.1

Support 40.2

EMI Part 47.1



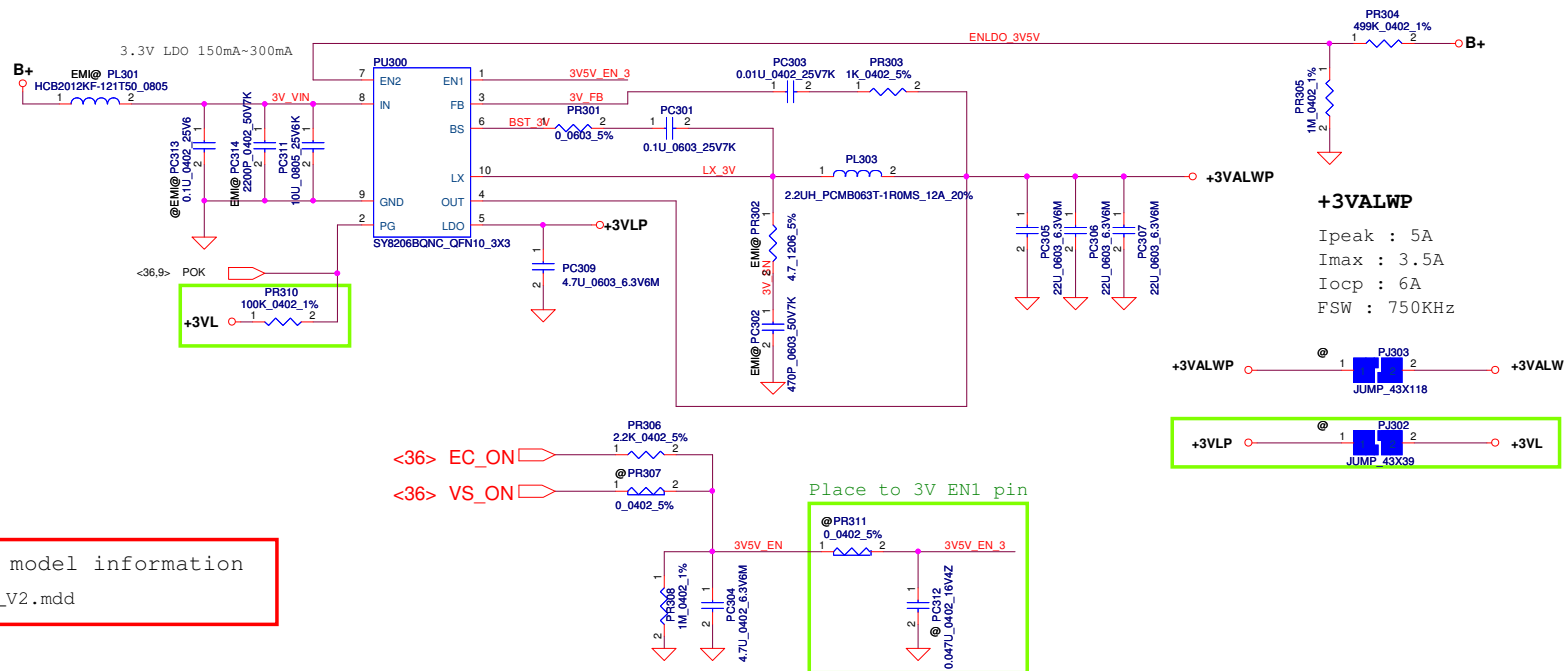
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b>	
Issued Date		Deciphered Date		Title	
				CHARGER	
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SY8206B\_V2.mdd

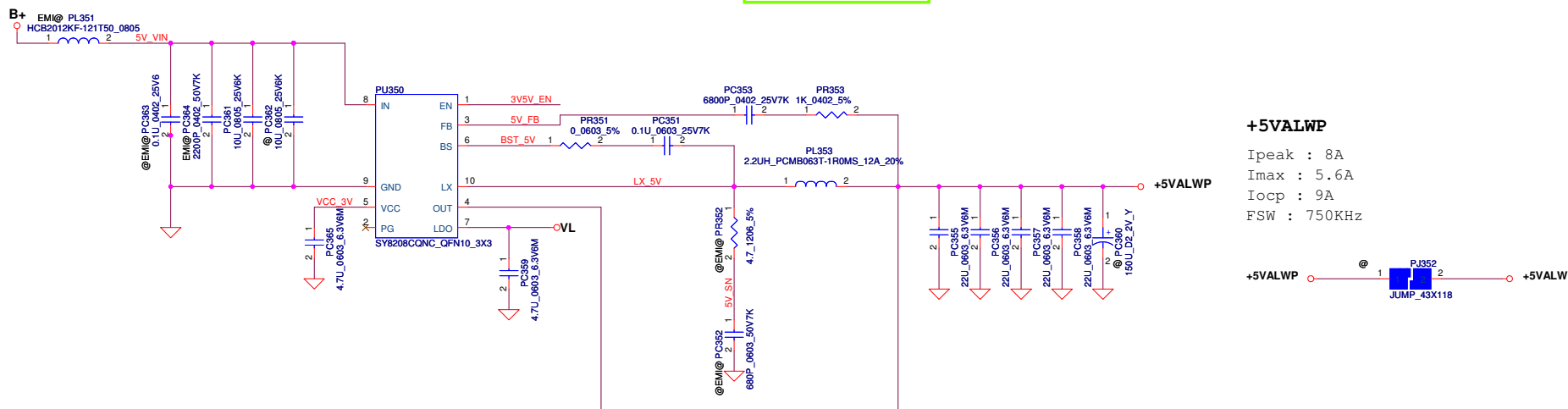
**Function Field :**

Support 35.2

EMI Part 47.1



SY8208C\_V2.mdd



Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> +3VALW / +5VALW	
Issued Date		Deciphered Date		Title +3VALW / +5VALW	
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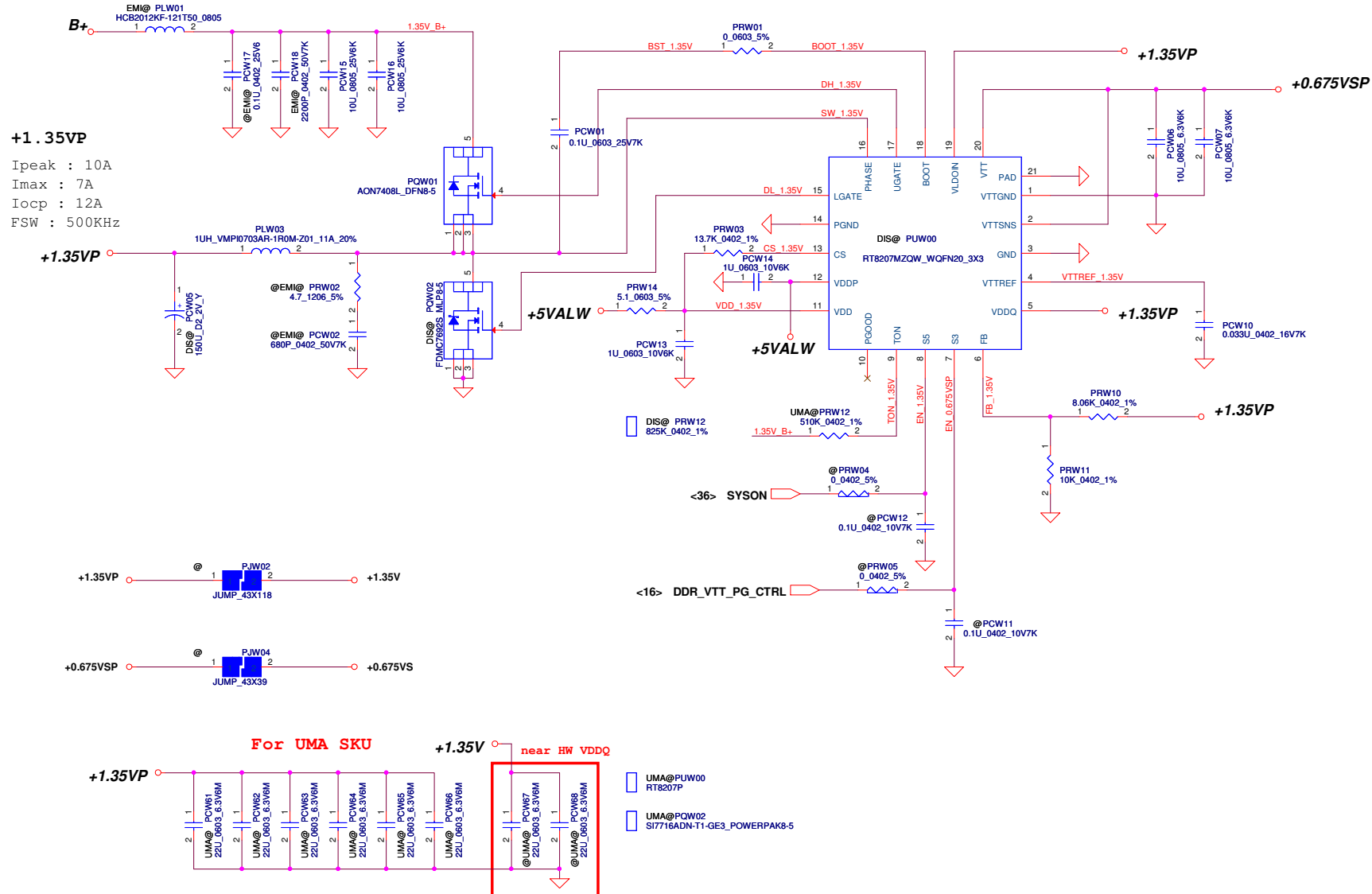
# Module model information

RT8207M\_V1.mdd For Single layer  
RT8207M\_V2.mdd For Dual layer

Mark Green frame that means this part is not belong to layout module part .

## Function Field :

Regulator 35.3  
Support 35.4  
EMI Part 47.1



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# Module model information

SY8206D\_V1.mdd

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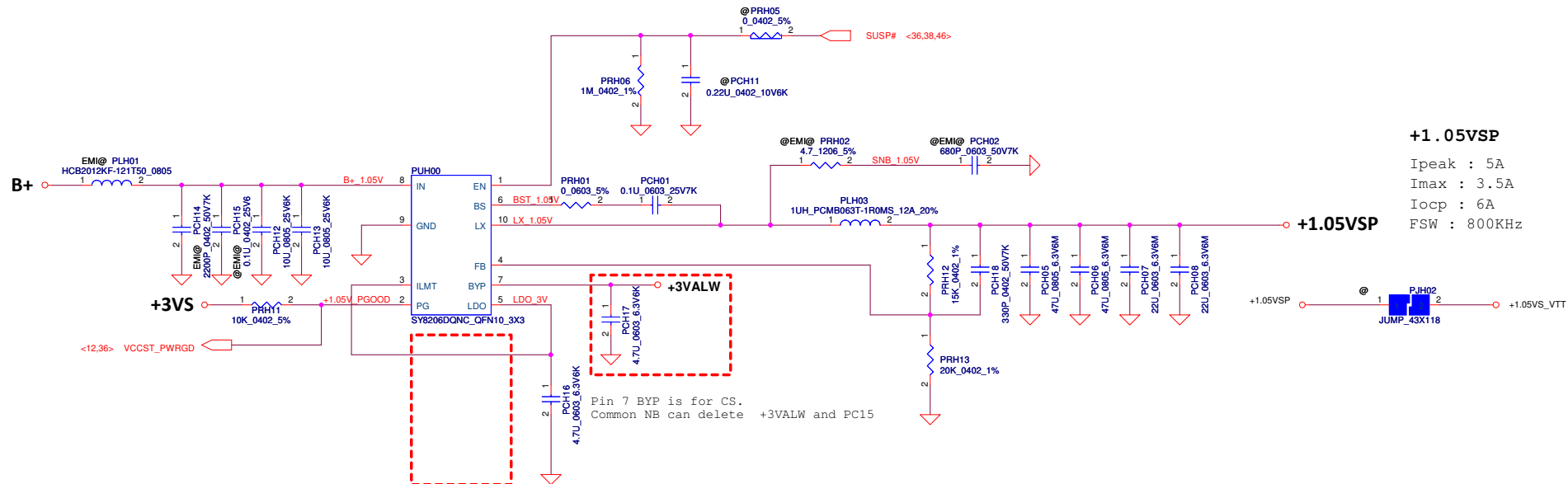
## Function Field :

Regulator 35.5

Support 35.6

EMI Part 47.1

EN pin don't floating  
If have pull down resistor at HW side, pls delete PR2



The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

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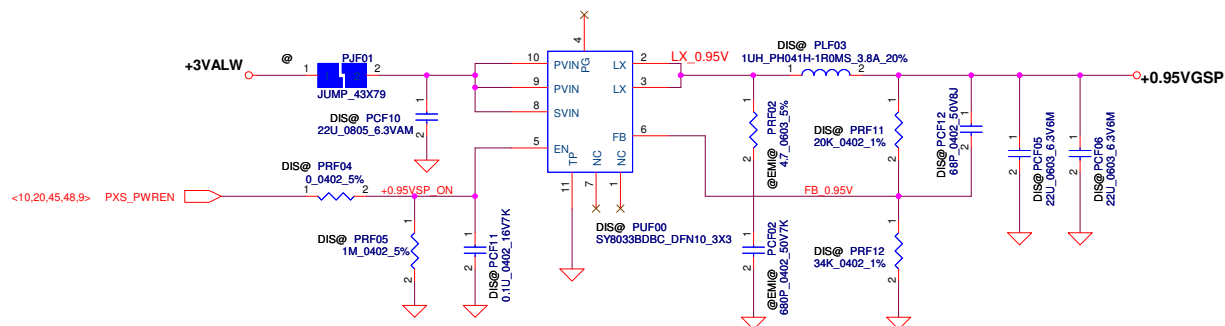
# Module model information

SY8033\_V1.mdd

Mark Green frame that means this part is not belong to layout module part .

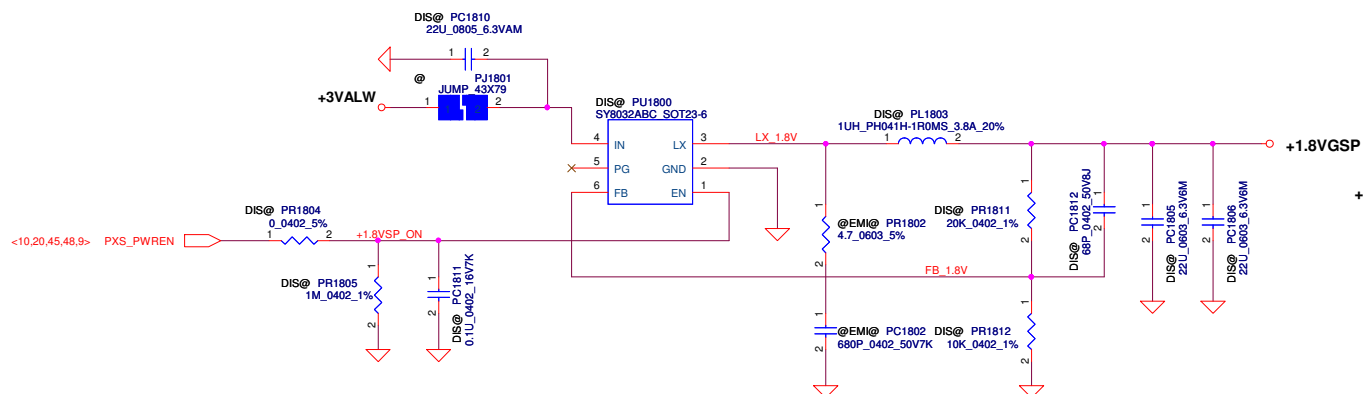
## Function Field :

Regulator 35.15  
Support 35.16  
EMI Part 47.1



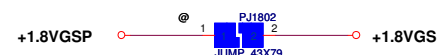
## +0.95VGSP

Ipeak : 3A  
Imax : 2.1A  
Iocp : 4A  
FSW : 1MHz



## +1.8VGSP

Ipeak : 1A  
Imax : 0.7A  
Iocp : 2.5A  
FSW : 1MHz



Note: Use VCCSA\_SEL to switch High & Low Level for VID[1]  
(ie. VCCSA\_SEL) due to the VID[0] is don't care for this setting.

Security Classification	Compal Secret Data		Title	
Issued Date		Deciphered Date	+0.95VGS / +1.8VS	
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Module model information

APL5930\_V1.mdd

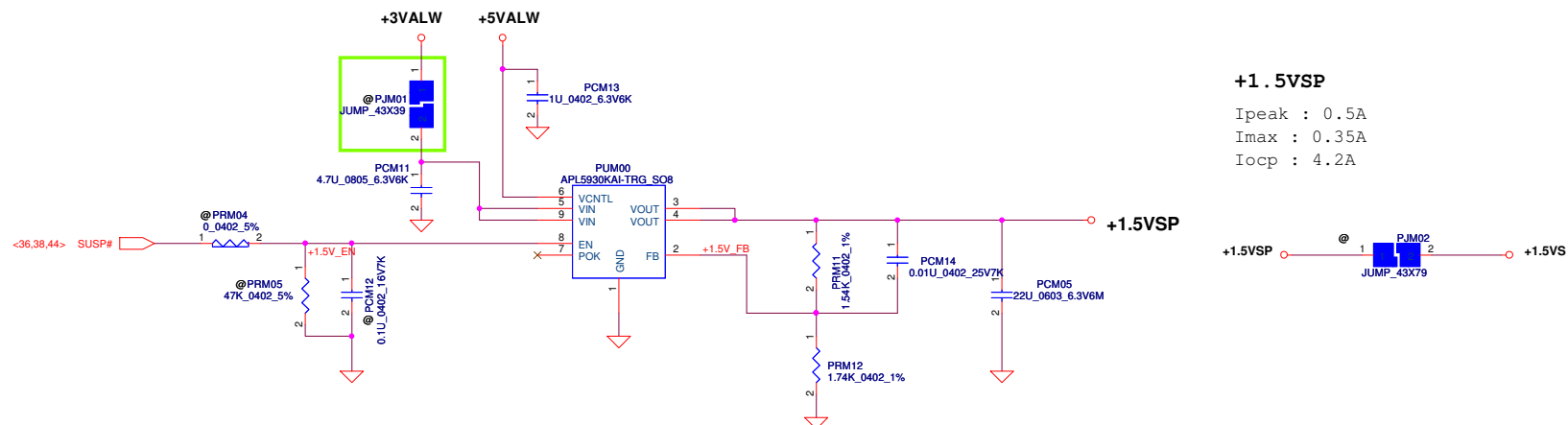
Mark Green frame that means this part is not belong to layout module part .

# Function Field :

Regulator 35.31

Support 35.32

EMI Part 47.1

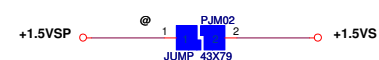


+1.5VSP

Ipeak : 0.5A

Imax : 0.35A

Iocp : 4.2A



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Issued Date		Deciphered Date		Title	+1.5VS	
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# Module model information

TPS51622\_V2A.mdd for IC portion  
TPS51624\_V2B.mdd for SW portion

## Function Field :

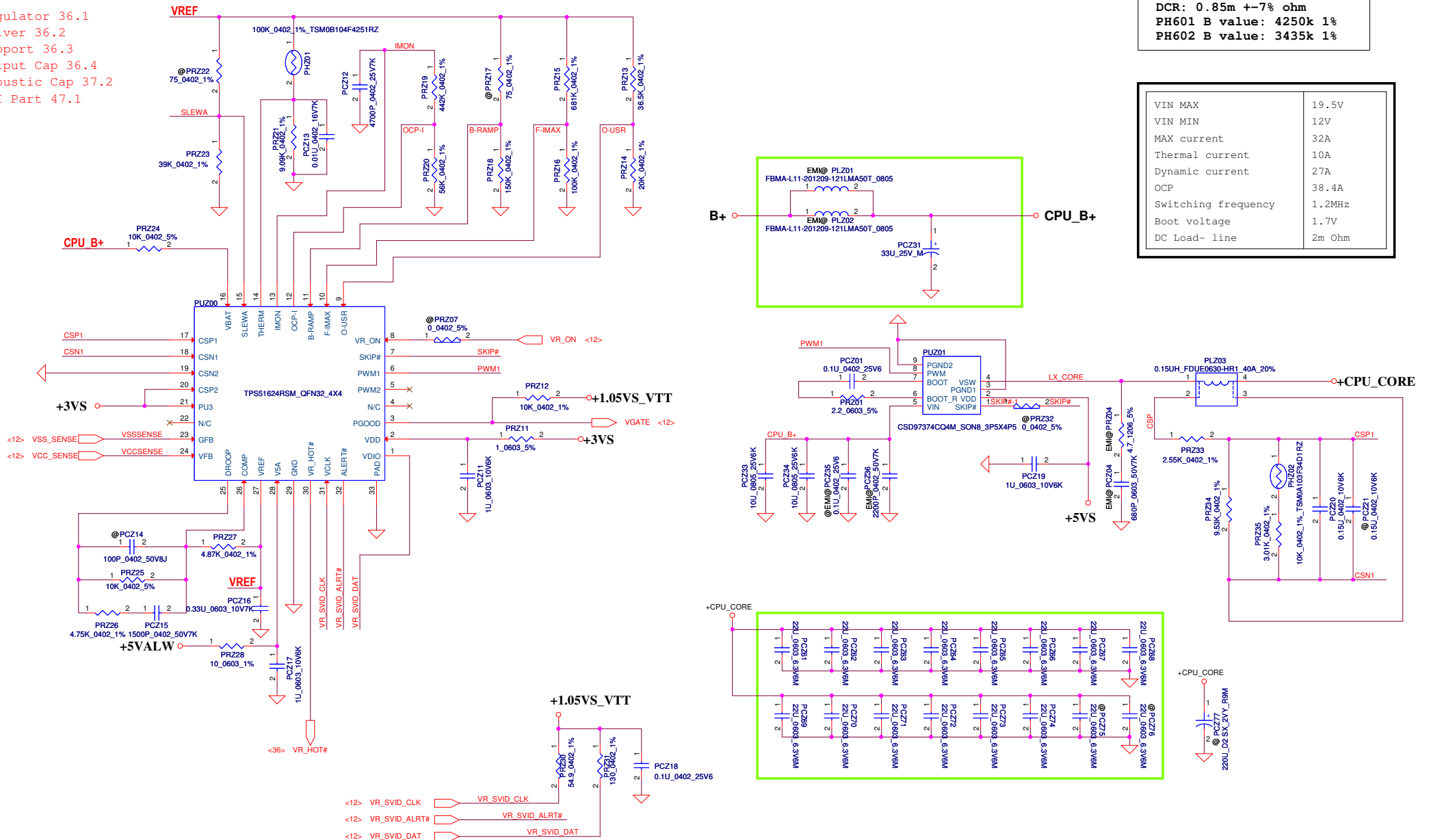
Regulator 36.1  
Driver 36.2  
Support 36.3  
Output Cap 36.4  
Acoustic Cap 37.2  
EMI Part 47.1

VR\_HOT#  
PR606 10K ohm for 100 degree  
PR606 8K ohm for 110 degree

Mark Green frame that means this part is not belong to layout module part .

CPU  
Frequency = 1MHz  
OCP Current 39 A  
DCR: 0.85m +-7% ohm  
PH601 B value: 4250k 1%  
PH602 B value: 3435k 1%

VIN MAX	19.5V
VIN MIN	12V
MAX current	32A
Thermal current	10A
Dynamic current	27A
OCP	38.4A
Switching frequency	1.2MHz
Boot voltage	1.7V
DC Load- line	2m Ohm



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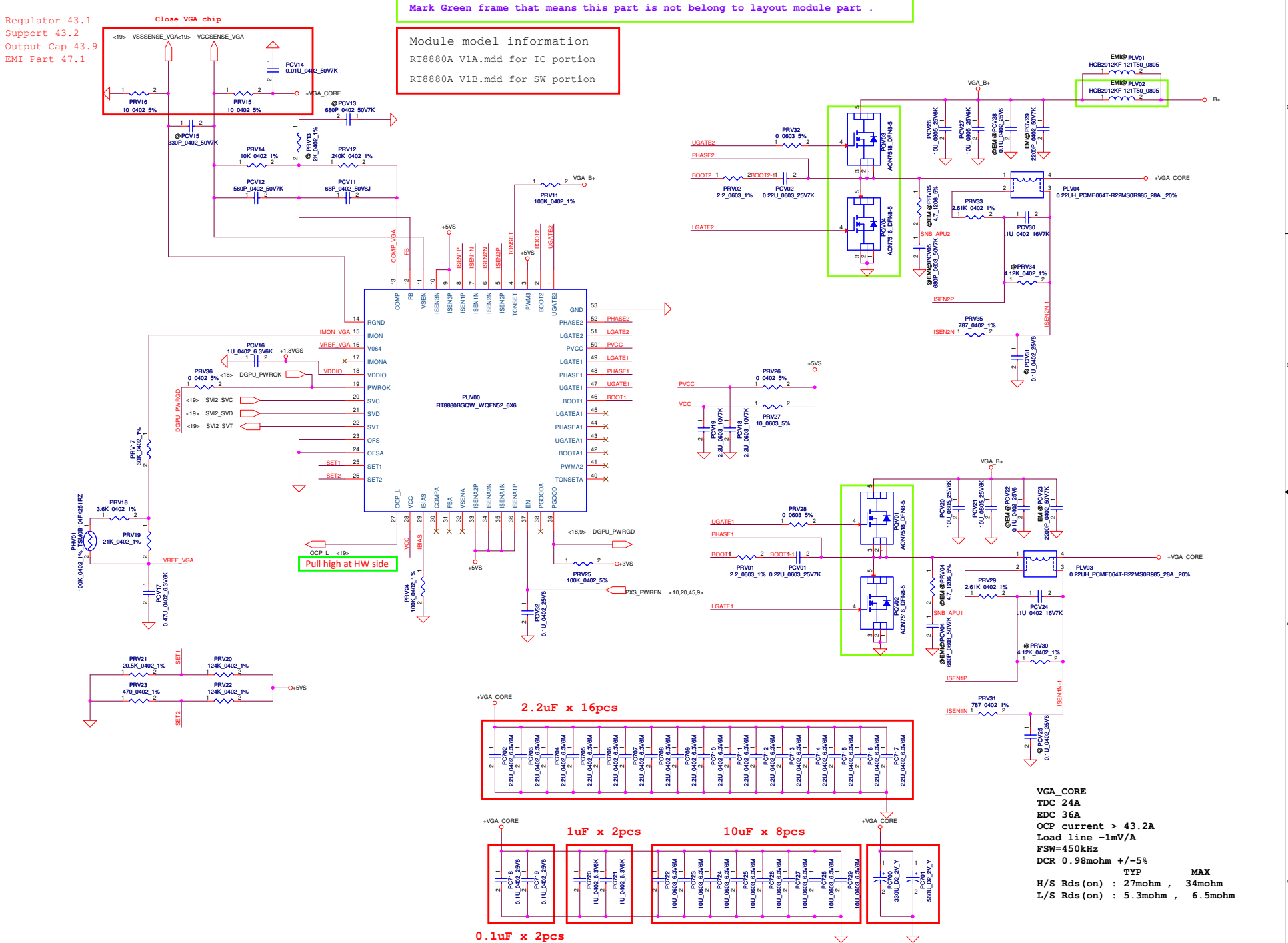
CPU\_CORE

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Function Field :

Regulator 43.1  
Support 43.2  
Output Cap 43.9  
EMI Part 47.1





## PWR PIR (Product Improve Record)

ZSWAA LA-B301P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.2

PVT GERBER\_OUT DATE: 2013/12/02

Item	Date	Page	Action	Component	Request
1)	11/21	48	Change	PRZ12 change to 10K and pull high +1.05VS_VTT	For design change
2)	11/21	48	Delete	PRZ29 removed	HW portion pull high
5)	11/25	41, 48	Change	PH1,PHZ01 part number change to SL200002H00	change for common PN
6)	11/25	48	Change	PHZ02 part number change to SL200002F00	change for common PN
7)	11/25	42	Change	change PQB03 to SB00000NW00 AON6414AL	change for allocation
8)	12/03	48	Change	PRZ27 change to 4.87K	change for compensation
9)	12/03	41	Change	PF2 change to 1206 footprint component SP040005P00	for ME limitation
10)	12/03	44	Change	change PQW02 to SB00000GW00 SI7716 at UMA SKU	change for allocation
11)	12/03	48	Change	PRZ19 change to 316K	for CPU core conversation fine tune
12)	12/03	48	Change	PRZ20 change to 56K	for CPU core conversation fine tune

REVISION CHANGE: 0.3

PV REGRESSION GERBER\_OUT DATE: 2014/01/06

Item	Date	Page	Action	Component	Request
13)	01/03	40	Change	change DC in jack footprint	for customer request
14)	01/03	43	Add	Add PR312 0ohm 0402	for HW 5V drop fine tune
15)	01/08	43	Change	change PR312 to 15ohm	for HW 5V drop fine tune
16)	01/08	47	Change	change PRZ19 to 442kohm	for CPU core conversation fine tune
17)	01/15	41	Delete	PCB10 2200p	for B2B fine tune
18)	01/15	41	Change	PCB11 0.1u change to 0.01u	for B2B fine tune
19)	01/16	43	Add	PR302,PC302 mount and PC302 change to 470p	for EMI request
20)	01/16	42	change	PCB16 2200p change to 0.047u	for decoupling cap fine tune
21)	01/22	47	Add	PRZ04,PCZ04 mount	for EMI request
22)	01/22	41	Add	PRB02,PCB02 mount	for EMI request
23)	01/22	47	change	PCZ31 100u change to 33u	for sourcer request

REVISION CHANGE: 1.0

Pre-MP GERBER\_OUT DATE: 2014/02/10

Item	Date	Page	Action	Component	Request
24)	02/07	42	Delete	remove PR312 15ohm	for HW request
25)	02/07	48	Change	change net name from VREF to VREF_VGA change net name from VREF to IMON_VGA change net name from VREF to COMP_VGA	resolve duplicate net name
26)	02/10	42, 44, 46	Change	change PR311,PRH05,PRM04 footprint to 0ohm shortpad	common design rule

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# HW PIR (Product Improve Record)

ZSWAA LA-B301P Schematic Change List

REVISION: 0.1

Gerber-out date: 2013/10/29

Item	Date	Page	Action	Component	Request
1)	10/15	37	Add	CB14 on SUSP#	For ESD request
2)	10/15	16,17	Change	Swap DDR data of JDIMM1 & JDIMM2	For common module layout
3)	10/15	08	Add	RH91 on CLK_REQ_VGA#	For follow AMD GPU reference schematic
4)	10/15	34	Reserve	CR6 to +5VALW	For power switch common design
5)	10/15	35	Add	CR2,CR3,CR5 to +USB_VCCB	For power switch common design
6)	10/16	37	Add	RB11,RB12	For colay EC 9022
7)	10/16	37	Add	RB13,RB14	For colay Normal pad & Click pad
8)	10/17	38	Add	R8,R9	For colay Normal pad & Click pad
9)	10/17	27	Add	R15,C29 on LCD_ENVDD	For tune LCD_VDD sequence
10)	10/18	34	Swap	LR9	For smooth USB signal
11)	10/18	37	Change	DFAN1 to Pin 70	For EC request
12)	10/20	34	Remove	RT2, RT3	For no need
13)	10/22	39	Change	RM5,RM6,RM7 to 0_0805	For max current design
14)	10/22	10	Add	Test point on GPIO10	For SW debug
15)	10/22	07	Add	Test point on GPIO34	For SW debug
16)	10/23	16	Reserve	0_0805	For DQA's experiment
17)	10/23	05	Change	R23 to 121_0402_1%	For Intel check list
18)	10/23	38	Remove	SW2	For layout space concern
19)	10/23	30	Reserve	RD11, RD12	For Intel check list
20)	10/24	08	Change	Y2 to 4 pin	For common part
21)	10/24	10	Add	RH4, RH6, RH9, RH10	For SW request
22)	10/24	26	Change	RT1 from 0603 to 0805	For current concern
23)	10/24	09	Add	RH7, RH8	For SW request
24)	10/24	27	Change	JTOUCH from 4pin to 6pin	For module pin define
25)	10/27	20	Change	QV5 to AO4354	For sourcer request
26)	10/27	34	Change	UT1 P/N to SA00007IO00	For TPM2.0

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# HW PIR (Product Improve Record)

ZSWAA LA-B301P Schematic Change List

REVISION: 0.2

Gerber-out date: 2013/12/2

Item	Date	Page	Action	Component	Request
01)	11/22	36	Delete	RA22	For audio codec
02)	11/22	36	Add	Add a reserve 0ohm resistor RA25	For EMI request
03)	11/22	27	Change	Change D15 P/N from SCS00002G00 to SCS00000Z00	For material shortage
04)	11/22	27, 29, 34, 35	Change	Change L10, L11, L62, L71, L72, L8, L9, LR7, LR8, LR9 P/N from SM070003Y00 to SM070003K00	For material shortage
05)	11/22	05	Change	Change R184 from SD013470080 to SD028470080	The same as CRB board
06)	11/26	26	Change	Change RT14 config. from @ to LVDS@	For BKOFF circuit
07)	11/26	09	Change	Change RH19 config. to IEDP@	For BKOFF circuit
08)	11/26	09	Connect	Connect EC_ENBKL_R_CPU to AND GATE U50.1	For BKOFF circuit
09)	11/26	27	Change	Change U50.1 from EC_ENBKL_R to EC_ENBKL_R_CPU	For BKOFF circuit
10)	11/26	27	Change	Change U50 and R433 config. from IEDP@ to always mount	For BKOFF circuit
11)	11/26	27	Change	Change D15 and R436 config. from LVDS@ to @	For BKOFF circuit
12)	11/26	36	Change	Change UB1.26 (EC GPIO12) from NC to TRANS_PRSNT	For BKOFF circuit
13)	11/26	36	Add	Add a pull high 10Kohm (RB23) to +3VL and a pull down 10Kohm (RB22) to GND on TRANS_PRSNT	For BKOFF circuit
14)	11/27	27	Change	Change D15 P/N from SCS00000Z00 to SCS0340L010	For BOM reduce
15)	11/27	29	Change	Change UD1.25, UD1.31, UD1.22, UD1.32 from +1.8VS_RXVCC to +1.8VS_CRT	For DP to CRT translator
16)	11/27	29	Change	UD1.45 pull high from +3VS to +3VS_6513	For DP to CRT translator
17)	11/27	29	Add	Add test point on UD1.37	For DP to CRT translator
18)	11/27	29	Add	Add RPD2 symbol for 150ohm	For DP to CRT translator
19)	11/27	33	Change	Change LAN/USB Small board Connector pin (JLAN.3 to JLAN.6) define	For LAN/USB Small board
20)	11/27	35	Change	Change UA1 all analog output net name to PR_L/PR_R	Unify net name
21)	11/27	35	Change	Change CA15 0.1u cap from 16V4Z to 10V7K	Don't need to use 16V4Z
22)	11/27	35	Change	Add net name Line1-L_C & Line1-L_R on UA1 pin 21.22	For trace length table
23)	11/27	35	Detete	Delete ALC233 co-lay component RA6, RA30, UA1	Change to ALC233VB Only
24)	11/27	35	Change	Swap RA21 & RA22 BOM structure	Balance caps alignment
25)	11/28	29	Change	Change test point T2 to a pull high 10Kohm (RD13) to +3VS_6513	For DP to CRT translator
26)	11/28	27	Add	Add a reserved ESD diode (D92) for JTOUCH	For ESD requeset
27)	11/28	07	Change	Change Dual ESD diode (D13) to two single diodes (D16, D17)	For RTC circuit
28)	11/28	07	Change	Change R437.1 connecting from +RTCBATT to +RTCVCC	For RTC circuit
29)	11/29	07	Change	Change R437 from 0ohm to 1kohm	For RTC circuit
30)	11/29	33, 37	Change	Change L56, L57 from SM070001U00 to SM070003K00	For EMI request
31)	11/29	33, 37	Change	Change L56, L57 from @EMI@ to EMI@	For EMI request
32)	11/29	33, 37	Change	Change R4, R5, R6, R7 from EMI@ to @EMI@	For EMI request
33)	11/29	34	Change	Change CR2, CR3, CR5 from 22U_0603 to 22U_0805	For droop issue
34)	11/29	35	Change	Change CA15 from SE076104K80 to SE102104K00	For BOM change
35)	11/29	07	Change	Change R277.2 net name from N113579902 to +RTCBATT_R	For RTC circuit
36)	12/01	33, 37	Change	Swap L56, L57 pin define	For layout request
37)	12/01	27	Add	Add R9, R11 on EMI camera choke	For EMI request
38)	12/01	27	Change	Change L62 from CAM_EMI@ to @CAM_EMI@	For EMI request

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# HW PIR (Product Improve Record)

ZSWAA LA-B301P Schematic Change List

REVISION: 0.3

Gerber-out date: 2014/01/06

Item	Date	Page	Action	Component	Request
01)	12/12	09	Change	Change RH19 BOM structure from IEDP@ to always mount	For LVDS & eDP cost down plan
02)	12/12	26	Change	Change RT14 BOM structure from LVDS@ to @	For LVDS & eDP cost down plan
03)	12/12	27	Delete	Delete U50,R433	For LVDS & eDP cost down plan
04)	12/12	27	Change	Change D15,R436 BOM structure from @ to always mount	For LVDS & eDP cost down plan
05)	12/12	36	Change	Change RB22 BOM structure from @ to IEDP@	For LVDS & eDP cost down plan
06)	12/12	36	Change	Change RB23 BOM structure from @ to LVDS@	For LVDS & eDP cost down plan
07)	12/12	07	Change	Change R277,D17 BOM structure from always mount to @	For RTC circuit
08)	12/12	07	Change	Change R437 BOM structure from @ to always mount	For RTC circuit
09)	12/30	11	Add	Add two reserved resistors R167,R168	For no use USB over current
10)	12/30	11	Change	Change UC1.AL3 connect to USB_OC#0_R	For no use USB over current
11)	12/30	11	Change	Change UC1.AH2 connect to USB_OC#2_R	For no use USB over current
12)	01/03	34	Add	Add a reserved capacitor CR7 on +USB_VCCB	For USB
13)	01/03	13	Add	Add a jumper PJ2 between +3VALW to +3VALW_PCH	For +3VALW to +3VALW_PCH
14)	01/06	38	Add	Add C549 and C550	For ESD's request
15)	01/06	37	Change	Change JLED footprint from E-T_6916K-Q06N-00L_6P to ACES_51524-0060N-001_6P	For DFX's request
16)	01/06	37	Change	Change JPWR footprint from E-T_6916K-Q04N-03R_4P to ACES_50504-0040N-001_4P	For DFX's request
17)	01/06	35	Change	Change UA1 Compal PN from SA00007BF00 to SA00007BF10	For audio codec
18)	01/07	13	Change	Change CH111,CH112,CH113,Q10,RH3 BOM structure from always mount to @	For +3VALW to +3VALW_PCH
19)	01/14	27	Change	Change D29 BOM structure from @ESD@ to ESD@	For ESD's request

ZSWAA LA-B301P Schematic Change List

REVISION: 1.0

Gerber-out date: 2014/02/10

Item	Date	Page	Action	Component	Request
01)	01/21	07, 09, 27	Change	Change D90,D91,D15,D16,D21,D17 from SCS0340L010 to SCS00003500.	For X code
02)	01/21	31	Change	Change JHDD footprint from SANTA_191503-1_22P-T to LCN_ASF98-2231S10-0002_22P.	For DFX's request
03)	01/21	37	Change/Add	Change CPU R1 BOM config and add R3 BOM config	For CPU BOM config
04)	01/29	33, 36	Add	Add a GPIO pin LAN_OFF# for UB1.25 and connected to JLAN.3	For Disable/Enable LAN chip
05)	01/29	36	Add	Add a GPIO pin PCH_RTCSRST#_R for UB1.18 and connected to a 0ohm resistor (RB29) and connected to PCH_RTCSRST#.	For RTC reset
06)	01/29	34	Add	Add a reserved capacitor 100uF (CR14) for +USB_VCCB.	For USB droop
07)	02/05	07, 09, 27, 35	Change	Change 0ohm resistor (RH19,R436,R32,R431,R432,RA11,RA1,RA2,RA10,R106) footprint to 0ohm short pad.	For 0ohm short pad
08)	02/05	35	Delete/Change	Delete RA13,RA18 and change UA1.18 to EXT_MIC and UA1.20 to +3VALW	For audio codec
09)	02/05	37	Change	Change SW3 BOM config from mount to un-mount.	For Pre-MP phase
10)	02/06	26, 27, 29, 35	Change	Change 0ohm resistor (RT1,RD1,LD2,RA20,RA21,R4280,R4281,R11,R9) footprint to 0ohm short pad, and BOM config to Rshort@.	For 0ohm short pad
11)	02/07	07, 09, 12, 27, 35, 16, 17, 36	Change	Change 0ohm resistor (RH19,R65,R178,R235,R174,R211,R212,R231,R436,LA1,LA3,RB34,RB1,R32,R431,R432,RA32,RA33,RA34,RA35,RA11,RA1,RA2,RA10,R106) BOM config to Rshort@.	For 0ohm short pad
12)	02/07	34	Delete	Delete CR7.	For USB droop
13)	02/07	38	Change	Change 0ohm resistor (RM3,RM5) footprint to 0ohm short pad, and BOM config to Rshort@.	For 0ohm short pad
14)	02/10	37	Change	Change screw hole size for H1,H2,H3.	For ME's request

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